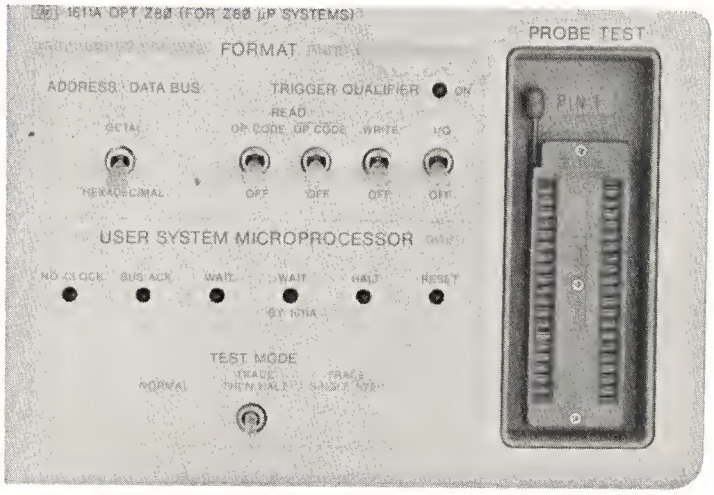
OPERATING AND SERVICE MANUAL SUPPLEMENT

1611A OPT Z80

(10260A) PERSONALITY MODULE FOR Z80 MICROPROCESSORS



HEWLETT PACKARD

HP Z80-1611A

SAFETY

This product has been designed and tested according to International Safety Requirements. To ensure safe operation and to keep the product safe, the information, cautions, and warnings in this manual, must be heeded. Refer to Section I and the Safety Summary for general safety considerations applicable to this product.

CERTIFICATION

Hewlett-Packard Company certifies that this product met its published specifications at the time of shipment from the factory. Hewlett-Packard further certifies that its calibration measurements are traceable to the United States National Bureau of Standards, to the extent allowed by the Bureau's calibration facility, and to the calibration facilities of other International Standards Organization members.

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For products returned to HP for warranty service, Buyer shall prepay shipping charges to HP and HP shall pay shipping charges to return the product to Buyer. However, Buyer shall pay all shipping charges, duties, and taxes for products returned to HP from another country.

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OPERATING AND SERVICE MANUAL
SUPPLEMENT

MODEL 1611A OPT Z80 (10260A) PERSONALITY MODULE FOR (Z80 MICROPROCESSORS)

SERIAL NUMBERS

This manual applies directly to instruments with serial numbers prefixed **1838A.**

With changes described in Section VII, this manual also applies to instruments with serial numbers prefixed **1830A.**

Manual Part Number 10260-90902
Microfiche Part Number 10260-90802

PRINTED: SEPTEMBER 1979

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SECTION I

GENERAL INFORMATION

1-1. INTRODUCTION.

1-2. This Manual Supplement contains: (1) information to install and test the Model 10260A; (2) operating information for the Model 1611A with Opt Z80 installed; (3) service information that complements service data in Section VIII of the 1611A Operating and Service Manual.

1-3. DESCRIPTION.

1-4. The Hewlett-Packard Model 1611A Option Z80 consists of a Z80 Personality Module installed in a 1611A standard mainframe for use with microprocessor based systems which use the Z80 (or equivalent) microprocessor.

1-5. The Model 10260A is available as an accessory to provide the Model 1611A Logic State Analyzer with Option Z80 capability.

1-6. SPECIFICATIONS.

1-7. Specifications for the Model 1611A with the Model 10260A installed are given in table 1-1.

1-8. RECOMMENDED TEST EQUIPMENT.

1-9. Equipment required to test the Model 10260A Option Z80 and verify its operation is listed in table 1-2. Other equipment may be substituted if it meets or exceeds the critical specifications listed in the table.

Table 1-1. Model 1611A Specifications (Model 10260A Installed)

CLOCK, DATA, ADDRESS, AND CONTROL INPUTS

CLOCK RATE: 500 kHz to 4 MHz.
INPUT CURRENT: -200 μA max, logic 0 (low); 20 μA max, logic 1 (high).
INPUT CAPACITANCE: approx 25 pF, includes capacitance of 30.4 cm (12 in.) cable; approx 15 pF with 7.6 (3 in.) cable.
THRESHOLD: 2 V minimum, logic 1 (high); 0.7 V maximum, logic 0 (low).

SETUP TIME

Data: 40 ns min relative to rising edge of $\overline{RD}$, $\overline{WR}$, or $\overline{IORQ}$.
Address: 200 ns min relative to rising edge of $\overline{RD}$, $\overline{WR}$, or $\overline{IORQ}$.

HOLD TIME

Data: 0 ns min relative to rising edge of $\overline{RD}$, $\overline{WR}$, or $\overline{IORQ}$.
Address: 0 ns min relative to rising edge of $\overline{RD}$, $\overline{WR}$, or $\overline{IORQ}$.
WAIT OUTPUT: TTL compatible open-collector output capable of sinking at least 8 mA when active.

EXTERNAL PROBE INPUTS

CURRENT: approx 50 μA logic 0 or logic 1.
CAPACITANCE: approx 25 pF at probe tip.
THRESHOLD: 2.4 V to 5.5 V, logic 1 (high); –0.8 V to 0.8 V logic 0 (low).
SETUP TIME: 150 ns min relative to rising edge of $\overline{RD}$, $\overline{WR}$, or $\overline{IORQ}$.
HOLD TIME: 0 ns, relative to rising edge of $\overline{RD}$, $\overline{WR}$, or $\overline{IORQ}$.

OUTPUTS

LOW: <0.4 V into 50Ω.
HIGH: >2.0 V into 50Ω (nominally 3.9 V into an open circuit).
TRIGGER: duration, approx 75 ns (RZ format); delay, approx 350 ns after the rising edge of $\overline{RD}$, $\overline{WR}$, or $\overline{IORQ}$ during the cycle that defines a valid trigger.
TRACE POINT (⌋⌈): provides a positive edge approx 350 ns after the rising edge of $\overline{RD}$, $\overline{WR}$, or $\overline{IORQ}$ that defines the specific valid trigger to be displayed on the 1611A. If the 1611A Delay is set so that the trigger word is not displayed, the Trace Point output occurs for the cycle that defines the valid word immediately preceding the first displayed word.
TRACE POINT (⌉⌊): complement of TRACE POINT (⌋⌈).

MICROPROCESSOR COMPATIBILITY

ZILOG: Z80
MOSTEK: Z80

Table 1-2. Recommended Test Equipment

Instrument	Critical Specification	Recommended Model	Use*
Pulse Generators (2)	10 V output into 50 ohms, External trigger, 0 to +2.5 V DC offset, 0 to 1.4 μs adjustable delay	HP 8012B	P
Digital Voltmeter	±1000 Vdc range, 0.1% accuracy	HP 3465A	A,T
Dual Channel Oscilloscope	100 MHz BW min	HP 1740A	P,T
Logic State Analyzer	Pattern recognition and state display	HP 1600A	T
Logic Pulser	Pulse logic circuits	HP 102526T	T
Logic Probe	Monitor digital IC's	HP 10525T	T
50Ω Feedthroughs (2)	50Ω feedthrough termination	HP 10100C	P
BNC-to-alligator Clip Adapter (2)		HP Part No. 8120-1292	P
Current Tracer	1 mA to 1A sensitivity	HP 547A	T
Signature Analyzer		HP 5004A or ET 9254	T

* P=Performance Test; A=Adjustment; T=Troubleshooting

SECTION II

INSTALLATION

2-1. INTRODUCTION.

2-2. This section contains information and instructions for installing the Model 1611A Option Z80 Personality Module.

2-3. Figures 2-1 and 2-2 are provided to facilitate component identification.

2-4. MODULE INSTALLATION. The 10260A consists of two printed circuit boards, a Z80 Personality Panel, and the dedicated Z80 Microprocessor Probe. To install the 10260A in an HP 1611A, preceed as follows:

a. Set LINE switch to OFF position and disconnect power cord.

b. Disconnect Microprocessor Probe A13 and External Probe A12 from rear panel.

c. Loosen captive screw on rear of 1611A top cover. Remove top cover and disconnect ribbon cable A11W2 from A9 (see figure 2-1).

d. Remove boards A5, A6, A7, A8, A9, and A10.

e. Disconnect ribbon cable A11W1 from connector A1P2 on Main Board A1 (see figure 2-2).

f. Remove screw that secures ground lug to A11 Board.

g. Remove two mounting screws that secure the A11 Board to Keyboard Support MP27 and remove A11 from instrument.

h. Place Option Z80 Personality Panel A11 in position and secure it with mounting screws removed in step g.

i. Secure ground lug to A11 as shown in figure 2-2.

CAUTION

Be sure that lug does not short to CRT mounting bracket.

j. Connect A11W1 into Main Board Connector A1P2 as shown in figure 2-2. Dot on main board indicates pin 1 of connector.

k. Install A10 Option Z80 ROM Board and A9 Option Z80 Personality Board onto Main Board A1 as shown in figure 2-1.

l. Connect A11W2 from Personality Panel to connector A9J1 on A9 board. Location of connector pin 1 is indicated by dot on board.

m. Reinstall A5, A6, A7 and A8 boards onto Main Borad A1 as shown in figure 2-1.

n. Connect new Option Z80 microprocessor probe A13 to A9 board through appropriate slot in rear panel and install two retaining screws.

o. Reconnect external probe A12 to A10 board through appropriate slot in rear panel and install two retaining screws.

p. Replace top cover to 1611A.

q. Reconnect power cord.

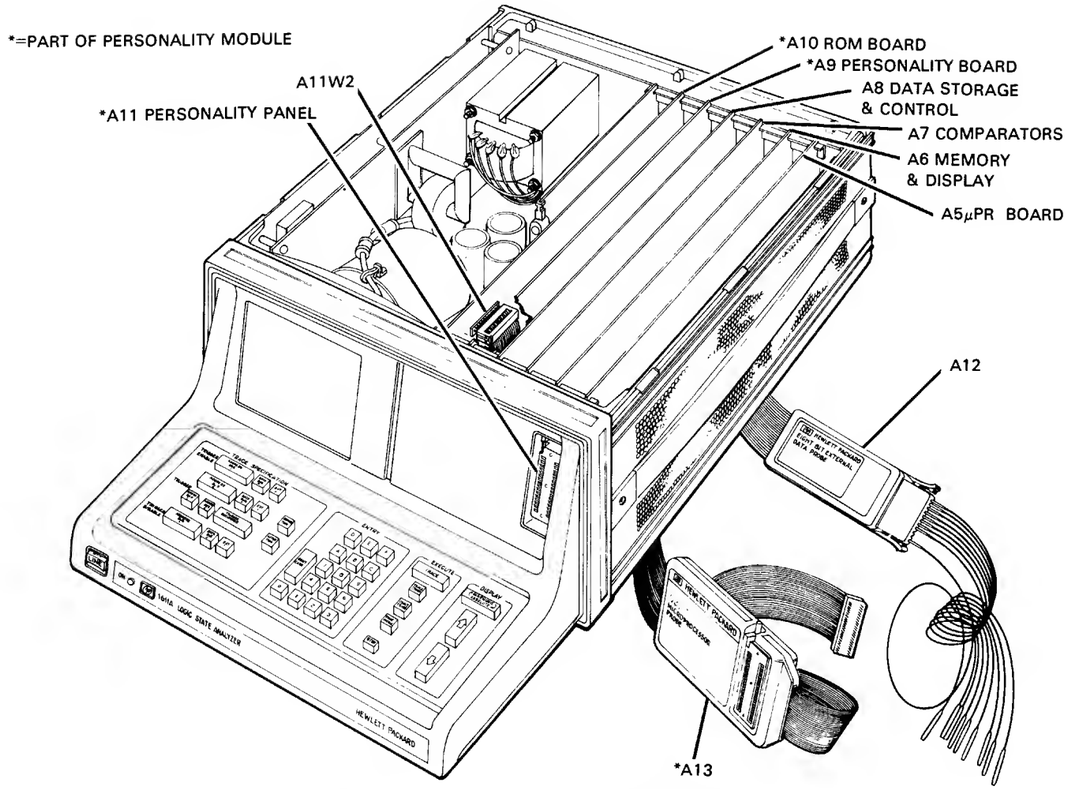


Figure 2-1. Model 1611A Assembly Locations

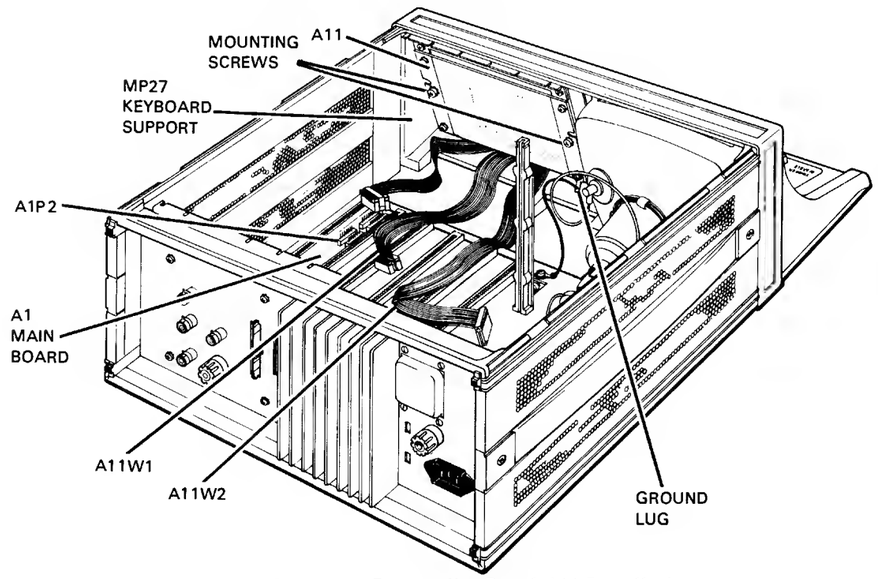
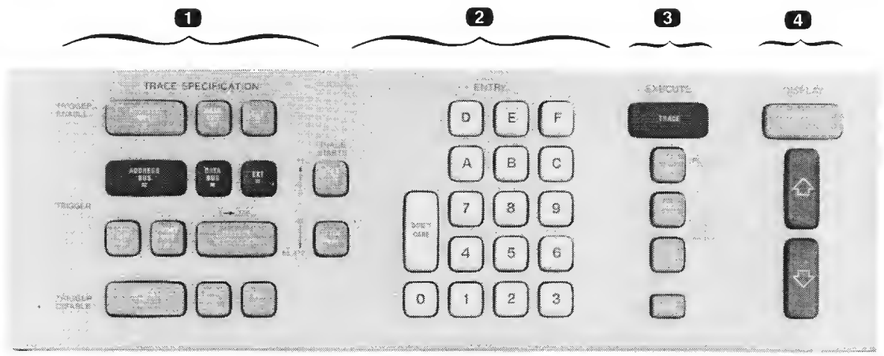
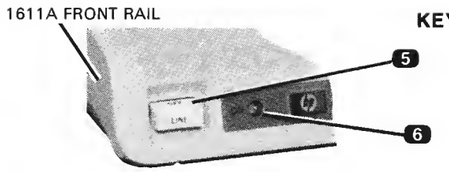


Figure 2-2. Personality Panel A11 Installation



KEYBOARD FEATURES



1 TRACE SPECIFICATION GROUP. Controls for setting up trigger conditions.

TRIGGER Keys.

ADDRESS BUS =. Opens field for entry of desired program or memory address trigger word. Entry is made with up to four hex or six octal characters and is automatically right-justified with leading zeros assumed.

DATA BUS =. Permits selection of 8-bit trigger word on data bus. Entries may be made with up to two hex or three octal characters and are automatically right-justified with leading zeros assumed.

EXT =. Permits trigger selection on eight lines from External Probe A12. Entry is made in binary and is automatically right-justified with leading don't cares assumed.

ADRS BUS ⩾ and ADRS BUS ⩽. These keys permit triggering to be limited to activity ⩾ or ⩽ selected address. Entry is made with up to four hex or six octal characters and is automatically right-justified with leading zeros assumed.

TRIGGER OCCURRENCE. Used to determine the number of trigger word occurrences before the trace starts. Entries of a decimal number $1 \leqslant n \leqslant 256$ are allowed. Trigger Occurrence is used only in TRACE mode. (If no entry is made, field assumes a value of 1.)

TRIGGER ENABLE and TRIGGER DISABLE Keys. Allow trigger recognition only after Enable and before Disable specifications are met.

ADDRESS BUS =. Controls trigger enable (or disable) recognition on program or memory address word. Entry is made with up to four hex or six octal characters and is automatically right-justified with leading zeros assumed.

DATA BUS =. Controls selection of an 8-bit trigger enable (or disable) word on data bus. Entries may be made with up to two hex or three octal characters and are automatically right-justified with leading zeros assumed.

EXT =. Controls trigger enable (or disable) recognition on eight lines from External Probe A12. Entry is made in binary and is automatically right-justified with leading don't cares assumed.

TRACE STARTS Keys. (TRACE mode only)

BEFORE TRIG. Selects number of memory transactions that trace starts before trigger (negative time or pretrigger). Entries are made with decimal number $n<63$.

AFTER TRIG. Selects number of memory transactions that trace starts after trigger (delay). Entries may be made with decimal number $n \leqslant 65472$. If no entry is made via Before or After Trig, field assumes value of 0.

2 ENTRY GROUP. Alphanumeric keys and DON'T CARE key for entering data into open sepcification field. Keeping DON'T CARE key depressed approximately three seconds clears all TRACE SPECIFICATION entries. If no open data field at the time, the message NO OPEN DATA FIELD will flash until the clear is completed.

3 EXECUTE GROUP. Instructs 1611A to perform a specific task or measurement.

TRACE. This mode provides for capture of 64 consecutive memory transactions in order to provide a display of microprocessor program execution.

TRACE TRIGGERS. In this mode, 1611A captures and displays only those memory transactions that match the preselected trigger conditions.

COUNT TRIGS. In this mode, 1611A counts trigger occurrences between Trig Enable and Trig Disable words.

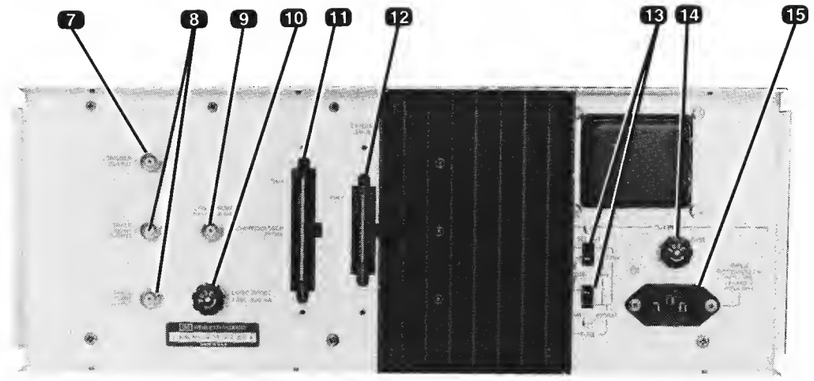
TIME INTERVAL. This mode produces read-out of elapsed time between two states defined by Trigger Enable and Trigger Disable. Timing measurement is made using an internal 1 MHz clock; accuracy is 0.1% ±1 μs.

STOP. Halts any execute function in progress; display of activity of μP system under test immediately prior to STOP command will result and STOPPED message will be displayed

4 DISPLAY GROUP. Used to conrol format of data displayed; keys do not change data stored in memory.

MNEMONIC/ABSOLUTE. Determines if data is displayed as captured (ABSOLUTE) or is to be inverse assembled into mnemonic statements with operands (MNEMONIC). In ABSOLUTE, each line of display represents one memory transaction which includes an address, data word, description of operation (e.g., op code, read, write), and eight external bits. In MNEMONIC, the data displayed often requires more than one memory transaction per line. The 1611A data display often contains less than 64 lines in MNEMONIC mode although data content is the same as in the 64-line ABSOLUTE display.

ROLL ↑ ↓. Used to roll 16-line display window through 64-byte memory.



REAR PANEL FEATURES

5 LINE. Line power switch.

6 ON. Indicator lights when line power is on.

7 TRIGGER OUTPUT⎍. Provides ~75 ns, RZ, TTL output on each occurrence of selected trigger word (useful for triggering test equipment).

8 TRACE POINT OUTPUT (⎍) (⎍). These outputs are levels which change state when a trace is initiated; they return to previous state when a trigger word is recognized or trace point is reached after delay. This provides a transition for triggering and a pulse for gating or causing breakpoints with external logic.

9 LOGIC PROBE. +5 V power connector for logic probes requiring less than 100 mA.

10 LOGIC PROBE FUSE. 500 mA fuse for Logic Probe Power.

11 MICROPROCESSOR PROBE. Microprocessor Probe Connector.

12 EXTERNAL PROBE. External Probe connector.

13 LINE SELECTOR. Slide switches for selecting 100-, 120-, 220-, or 240-Vac line operation.

14 FUSE. Use 1.0 AT time-delay fuse for 100-, 120-Vac operation; 800-mAT time-delay fuse for 220 or 240-Vac operation.

15 POWER INPUT. Power cable connector.

1 NO CLOCK. I
microprocesso
clock period i
μs.

2 BUS ACK. I
output is LO.

3 WAIT. Indica

4 TEST MODE
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TRACE TRI
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TRACE SING
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TRACE exec
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5 WAIT BY 161
generated by
TRACE SIN

6 HALT. Indica
put is LO.

7 RESET. Indi
input is LO.

8 PROBE TEST
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9 TRIGGER QU
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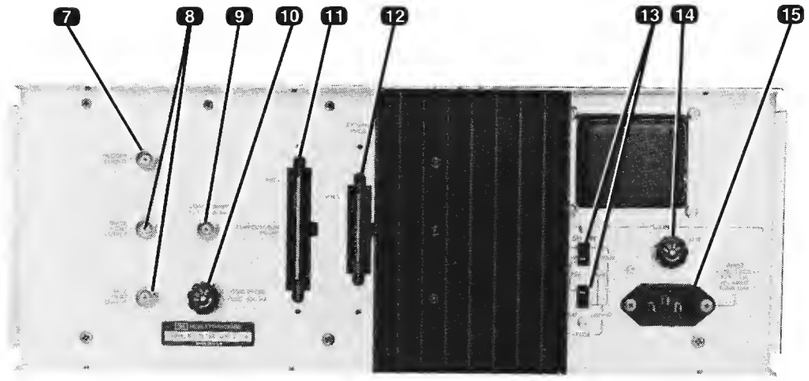
Figure 3-1.
Keyboard and Rear Panel Features



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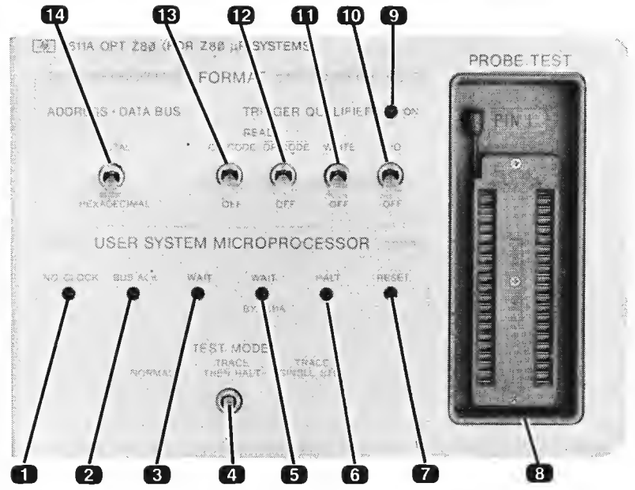


1 NO CLOCK. Light is on when no Φ clock from microprocessor under test is present or when Φ clock period is greater than approximately 100 μs.

2 BUS ACK. Indicates that Z80 CPU $\overline{\text{BUSAK}}$ output is LO.

3 WAIT. Indicates Z80 CPU WAIT Input is LO.

4 TEST MODE.
NORMAL. Data is captured and displayed with microprocessor under test operating without interruption of program flow.
TRACE THEN HALT. 1611A executes TRACE or TRACE TRIGS, and when data acquisition is completed, places microprocessor under test in Halt state.
TRACE SINGLE STEP. Only one instruction cycle is processed and displayed during each TRACE execution. 1611A halts microprocessor under test after each instruction cycle.

5 WAIT BY 1611A. Indicates when wait state is generated by 1611A in TRACE THEN HALT or TRACE SINGLE STEP mode.

6 HALT. Indicates that the Z80 CPU HALT output is LO.

7 RESET. Indicates that the Z80 CPU RESET input is LO.

8 PROBE TEST. Test socket for microprocessor probe; provides test pattern to Probe A13 for testing most system functions and controls.

9 TRIGGER QUALIFIER. Indicates that Trace Specification (including TRIGGER, ENABLE, and DISABLE) must occur during a specific type of machine cycle before 1611A trigger will occur. When trigger requirements are satisfied via Trigger Qualifiers, a TRACE measurement proceeds normally (Before or After Trigger specification and data acquisition are not affected). If all switches are in OFF position, the 1611A will trigger on any machine cycle that meets Trace Specificaion requirements.

10 I/O. Allows 1611A trigger to occur on Input/Output machine cycles.

11 WRITE. Allows 1611A trigger to occur on Memory Write machine cycles.

12 READ $\overline{\text{OP CODE}}$. Allows 1611A trigger to occur on Memory Read machine cycles other than Op-Codes.

13 READ OP CODE. Allows 1611A trigger to occur on Op-Code Fetch machine cycles.

NOTE

Any combination of QUALIFIER switches may be used to allow the 1611A trigger to occur on more than one type of machine cycle.

14 OCTAL/HEXADECIMAL. Selects octal or hexadecimal format for data display and Trace Specifications. Flashing symbols (?) are displayed in Trace Specification field when a specification contains "don't cares" in octal or hexadecimal format, and switch is then placed in opposite position. Binary and decimal numbers are unaffected.

Figure 3-2. Personality Panel Controls and Indicators

SECTION III

OPERATION

3-1. INTRODUCTION.

3-2. This section provides operating information, explains functions of 1611A controls, connectors, and indicators, and describes measurement capabilities and operating characteristics of the 1611A with a Model 10260A Option Z80 installed.

3-3. PANEL FEATURES.

3-4. Keyboard and rear-panel features are shown in figure 3-1. Personality Panel A11 is shown and described in figure 3-2.

3-5. PROBES. The 1611A uses two probes to acquire data from the system under test. Primary Probe A13 is dedicated to the microprocessor and is not interchangeable with other 1611A options. It gathers signals from the microprocessor Address and Data busses along with the clock and control signals. Connection is made from the probe pod to the microprocessor socket in the system under test through a ribbon cable and connector. The pod contains a socket for the microprocessor. If the microprocessor cannot be removed from the system, the connector cable and plug can be replaced with a ribbon cable terminated with a dual in-line clip connector which provides a direct connection from the pod to the microprocessor. When the clip is used, the socket on the probe pod is left empty.

3-6. The external probe A12 is secondary, with no clock input, and is not required for instrument operation. It has eight uncommitted input lines to accept data coincident with data bus inputs on the primary probe. Input impedance is approx 1 MΩ shunted by ≤25 pF at the probe tip.

3-7. SETTING TRACE SPECIFICATIONS.

3-8. At instrument turn on, the display should be as shown in figure 3-3. The display is divided into two parts by a dashed horizontal line. Above this line, all pertinent trace specifications are displayed as they are entered. The trigger ADDRESS bus field is open (inverse video field to right of TRIGGER). A blinking cursor in the lower left corner of the field indicates where a character entered by means of the ENTRY key group will be located.

3-9. The first step in making a measurement is to set up the trace specification. Pressing the key for the desired specification in the TRACE SPECIFICATION key group opens the data field. This field is now ready to accept data from the ENTRY key group for ADDRESS (Octal or Hex), DATA (Octal or Hex), or EXTERNAL (Binary only) specifications.

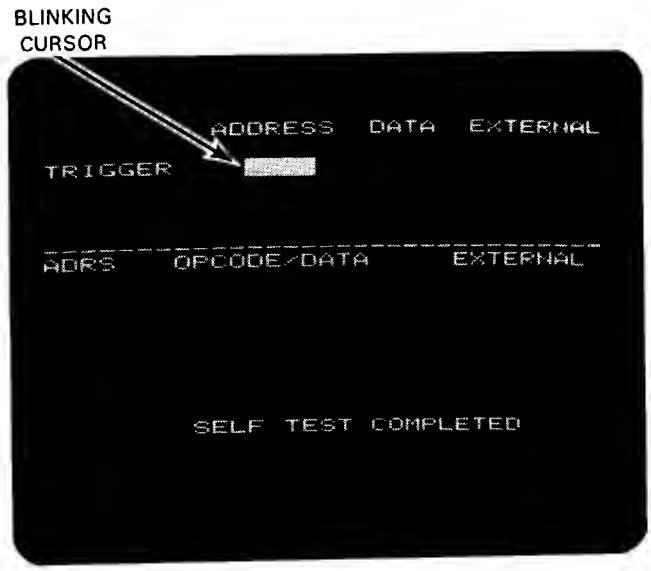


Figure 3-3. Turn-on Display

3-10. To enter data in the field, key in the desired value. If the pressed key is an illegal character for the selected specification field (such as an alpha character for a decimal field), an ILLEGAL CHARACTER message is flashed on the display. This message is cleared when the ENTRY key for an acceptable character is pressed, or when a new TRACE SPECIFICATION, EXECUTE, or DISPLAY field key is selected. All entries are automatically right-justified, and any EXTERNAL entries automatically assume leading don't cares, while ADDRESS and DATA entries automatically assume leading zeros.

3-11. An existing trace specification can be changed or deleted in the following manner. To change a trace specification, press the TRACE SPECIFICATION key for that field, then enter the new data. To delete a trace specification, press the TRACE SPECIFICATION key for that field, then press DON'T CARE in the ENTRY key group. All TRACE SPECIFICATION fields can be "cleared" by pressing DON'T CARE key for approximately three seconds.

3-12. TRIGGERING. The TRIGGER keys ADDRESS BUS =, DATA BUS =, and EXT =, can be used in any combination to specify a 1611A trigger word. ADDRESS BUS = key allows 1611A to trigger on a desired μP program or memory address word. DATA BUS = key allows 1611A to trigger on a desired μP data bus word.

EXT = key allows 1611A to trigger on a desired external word. When more than one key is used, all requirements must be satisfied. The TRIGGER ENABLE field allows the 1611A to recognize only those triggers which occur after the Enable specification has been detected. The TRIGGER DISABLE field allows the 1611A to recognize only those triggers which occur before the Disable specification has been detected. When used together, the Enable and Disable fields define a window, in which the 1611A is allowed to search for specified triggers. The ADDRS BUS ≥ key allows any address bus value which is greater than or equal to the value specified (from the value specified up to $FFFF_{16}$ or 177777_8) to be recognized as a trigger. The ADDRS BUS ≤ key allows any address bus value which is less than or equal to the value specified (from the value specified down 0000_{16} or 000000_8) to be recognized as a trigger. These two keys may be used together to define ranges over which any address bus activity will generate a trigger. For example, if a smaller number is entered in ≥ field than is entered in the ≤ field, then only the address bus activity within this window will be recognized. If a larger number is entered in ≥ field than is entered in the ≤ field, then the address bus activity which occurs outside of this window will be recognized and displayed. Trigger requirements, including Enable and Disable, can be restricted to particular μP machine cycles with the TRIGGER QUALIFIER switches on Personality Panel A11.

3-13. TRACE MEASUREMENT EXECUTION.

3-14. TRACE. This is the most common mode of data acquisition. Trace mode allows capture of up to 64 consecutive memory transactions from the microprocessor system under test. After a completed Trace measurement run, the 1611A high-speed memory contains up to 64 memory transactions. The memory transactions are viewed through a 16-line movable window (figure 3-4). Thus, in Trace mode the 1611A can monitor and display the program execution of the microprocessor system under test.

3-15. The starting point for data acquisition is selected via the TRIGGER, TRIGGER OCCURRENCE, and BEFORE or AFTER TRIG Keys. The TRIGGER OCCURRENCE requirement will allow the 1611A to recognize the trigger only on the nth occurrence (with n being any desired value from 1 to 256; if no entry is made, field assumes a value of 1). The BEFORE TRIG Key can be used to start the trace up to 63 words before the trigger. This permits viewing of events leading up to the trigger (negative-time or pretrigger). The AFTER TRIG Key can be used to delay start of the trace up to 65 472 transactions after the Trigger event (figure 3-5). When AFTER TRIG delay is used, the data captured in high-speed memory will not contain the Trigger word.

3-16. Trace display may be viewed in ABSOLUTE or MNEMONIC mode. In both modes the program or memory address is displayed in the ADRS column. In ABSOLUTE (figure 3-6), the machine language op-code or data and the type of μP machine cycle (e.g., READ),

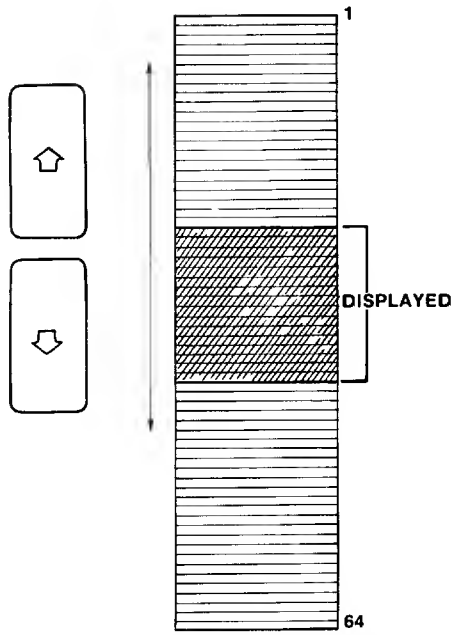


Figure 3-4. Display Window

OPCODE, WRITE) are displayed in the OPCODE/DATA column (table 3-1). In MNEMONIC, the assembly language mnemonic and 8 or 16 bit operand (if the operand exists) are displayed in the OPCODE/DATA column (figure 3-7). If an invalid op-code is detected, then *** will be the flashing in the OPCODE/DATA column when in MNEMONIC MODE. IF *'s are displayed NOT flashing then the operand was not captured by high-speed memory. Hexadecimal or octal format can be selected and interchanged in both display modes.

Table 3-1. Z80 Memory Transactions Displays

OPCODE	The contents of the data bus is an op-code.
OPCODE 2	The contents of the data bus is the second or third byte of a multi-byte op-code.
WRITE	The contents of the data bus is information being written to memory.
READ	The contents of the data bus is being read from memory.
INPUT	The contents of the data bus was read from an I/O port.
OUTPUT	The contents of the data bus is data to be written to an I/O port.
INTR	The data bus contains an interrupt vector from an interrupting device.

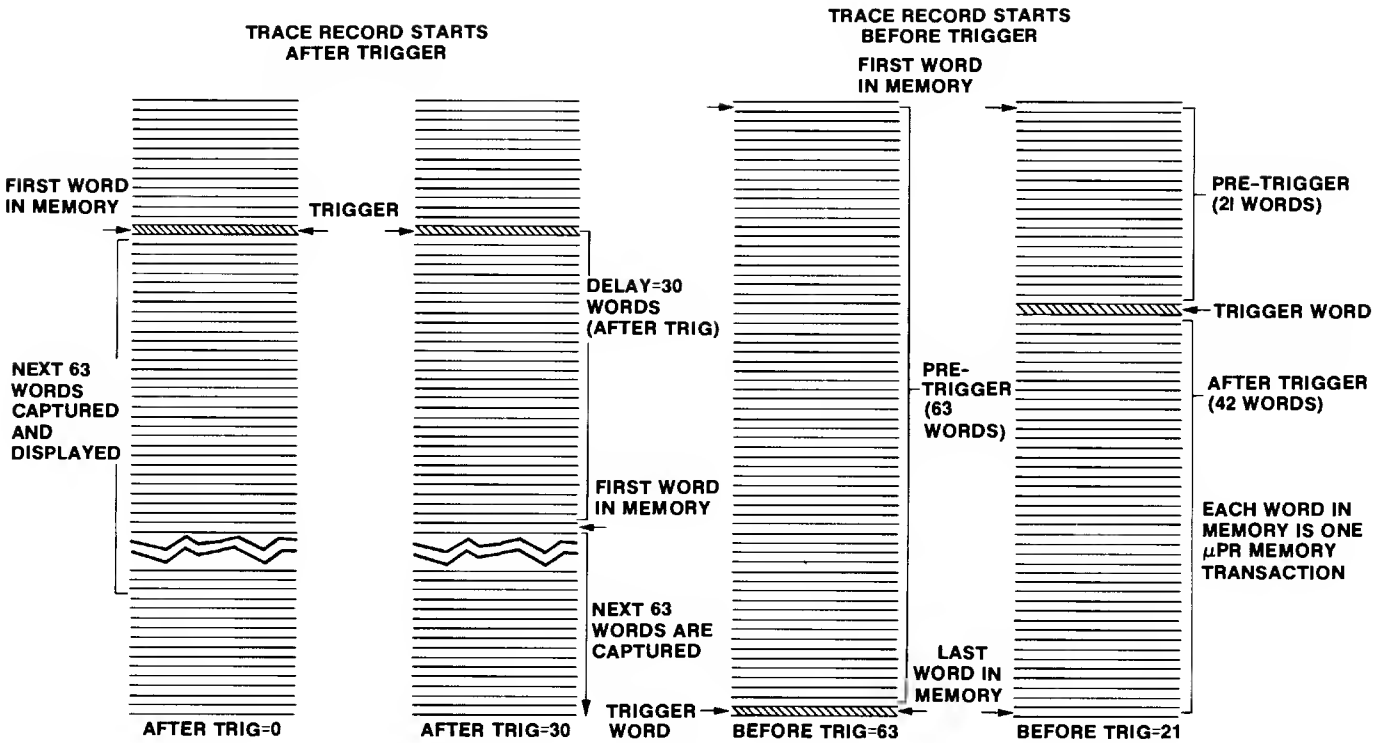


Figure 3-5. After Trigger and Before Trigger Displays

```
                ADDRESS   DATA   EXTERNAL

TRIGGER         001C

                                    LINE   0
ADRS    OPCODE/DATA              EXTERNAL
001C    DD    OPCODE             0000 0000
001D    E1    OPCOD2             0000 0000
0101    00    READ               0000 0000
0102    01    READ               0000 0000
001E    FD    OPCODE             0000 0000
001F    22    OPCOD2             0000 0000
0020    00    READ               0000 0000
0021    01    READ               0000 0000
0100    01    WRITE              0000 0000
0101    01    WRITE              0000 0000
0022    FD    OPCODE             0000 0000
0023    2A    OPCOD2             0000 0000
0024    00    READ               0000 0000
0025    01    READ               0000 0000
0100    01    READ               0000 0000
0101    01    READ               0000 0000
```

Figure 3-6. Absolute Mode Display

```
                ADDRESS   DATA   EXTERNAL

TRIGGER         001C

                                    LINE   0
ADRS    OPCODE/DATA              EXTERNAL
001C    POP  IX                  0000 0000
0101      00   READ              0000 0000
0102      01   READ              0000 0000
001E    LD (0100),IY             0000 0000
0100      01   WRITE             0000 0000
0101      01   WRITE             0000 0000
0022    LD IY,(0100)             0000 0000
0100      01   READ              0000 0000
0101      01   READ              0000 0000
0026    PUSH IX                  0000 0000
0102      01   WRITE             0000 0000
0101      00   WRITE             0000 0000
0028    SUB (IY+02)              0000 0000
0103      FF   READ              0000 0000
002B    AND (IX+04)              0000 0000
0104      00   READ              0000 0000
```

Figure 3-7. Mnemonic Mode Display

3-17. Trace measurements may be made in NORMAL, TRACE THEN HALT, or TRACE SINGLE STEP mode. These modes are selected by the TEST MODE switch on Personality Panel A11. In NORMAL, the 1611A captures and displays data while the microprocessor system under test operates without interruption of program flow. In TRACE THEN HALT, the 1611A places the μP system under test in a Halt state when the data acquisition cycle is completed. In TRACE SINGLE STEP, the 1611A Halts the μP system under test after each instruction cycle. The SINGLE STEP mode is functional only in TRACE measurements. During each TRACE execution only one μP instruction cycle is processed and displayed.

3-18. A TRACE measurement is initiated each time the TRACE key is pressed. Repeated TRACE runs may be made with continuous-run execution. Continuous execution is initiated by pressing TRACE key approximately two seconds. The message CONTINUOUS will be displayed. Pressing the TRACE key again restores regular operation. Continuous runs may be stopped by pressing STOP key or aborted by pressing any other key.

3-19. TRACE SETUP. Enter TRIGGER requirements. Any desired combination of Trigger Enable, Trigger Disable, Trigger Occurrence, and Before or After Trigger requirements may be entered. Ranges of address bus values which will be recognized as Triggers may also be entered with ADDRS BUS $\geq$ or $\leq$ keys. Triggering (including Enable and Disable) may be restricted to certain types of μP under test machine cycles with the TRIGGER QUALIFIER switches on Personality Panel A11. Press TRACE key.

3-20. Display in TRACE.

3-21. Before the first trigger is detected, two messages may be displayed: (1) WAITING FOR ENABLE flashes until the Enable specification (if entered) is detected; (2) WAITING FOR TRIGGER flashes until the Trigger specification is detected (after the Enable, if specified, has been detected).

3-22. WAITING FOR ENABLE and WAITING FOR TRIGGER can be alternating. This happens when both Enable and Disable are specified and no trigger is found in the window. The Enable is found, no trigger is found, the Disable is found, and the 1611A looks for another Enable.

3-23. After the first Trigger is detected, but before the TRACE measurement is complete, two messages may be displayed: (1) TRIGR OCCUR = shows how many Triggers are detected from the first Trigger until the Trigger Occurrence specification is met; (2) DELAYING is shown from the time Trigger Occurrence specification is met until the measurement is complete.

3-24. Any data shown below the dashed line will not change until the measurement is complete or until data acquisition is stopped by the STOP key. When a measurement is completed, the Trigger word is shown in an inverse video field, if no AFTER TRIGGER DELAY is specified (figure 3-8). The message LINE 0 also appears. The DISPLAY ROLL keys may be used to move the 16-line display window through the 64 lines (0 to 63) stored in high-speed memory. The LINE message will vary from 0 up to 48. The LINE number shown is the number of the top line in the 16-line display (48 + 15 = 63).

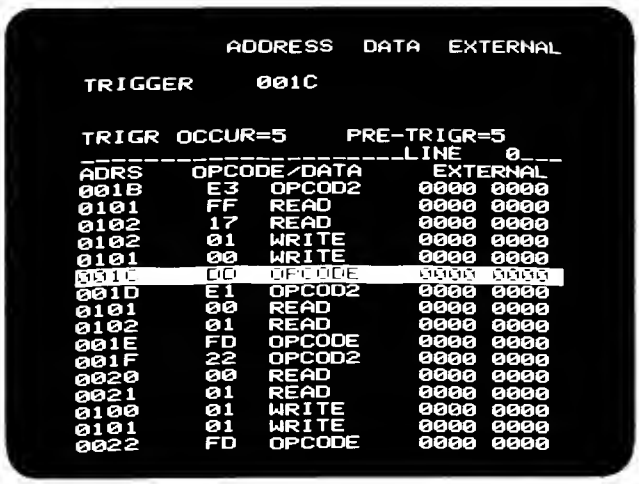


Figure 3-8. Trace Display

3-25. IF an incomplete TRACE measurement is stopped by the STOP key, then all data acquired by the high-speed memory during measurement will be displayed (memory dump). If the memory has no new data, then the data display section will be blank. The message STOPPED is shown.

3-26. When a TRACE measurement is incomplete and any key other than an EXECUTE key is pressed, the measurement run is aborted. The display remains as it was before the measurement. Any attempt to change the display with DISPLAY group keys will result in the message RUN ABORTED, NO DISPLAY CHANGE.

3-27. Partial displays (less than 64 memory transactions stored for display) can occur in Trace mode when using a BEFORE TRIGGER specification. The minimum number of lines that will be displayed in ABSOLUTE mode is 64 minus the BEFORE TRIG specification. Internally, the 1611A completes a measurement by counting the number of memory transactions after the Trigger. Because of this, the 1611A may not display the number of memory transaction BEFORE TRIG that have been specified. If a BEFORE TRIG entry of 60 is made, then the 1611A will terminate the measurement 3 memory transactions after the Trigger. This allows for up to 60 memory transactions before the Trigger, the Trigger, and 3 memory transactions after the Trigger to be captured in high-speed memory. If, after the Trace measurement was started, the system under test exe-

cuted only 15 memory transactions before the Trigger occurred, then the 1611A would display only 19 memory transactions. The ROLL keys can be used to view the 15 transactions before the Trigger, the Trigger, and 3 transactions after the Trigger. The display will not roll up any further once the last memory transaction captured by the 1611A is in the bottom line of the display.

3-28. TRACE TRIGGERS MEASUREMENT EXECUTION.

3-29. TRACE TRIGGERS. In this mode the 1611A captures and displays only memory transactions that match the Trigger specification. For example, the operator may want to see only "Write" operations from a block of memory to verify that proper data was entered. This is easily done by using the Write TRIGGER QUALIFIER switch on Personality Panel A11. The run automatically terminates when 64 Triggers have been found. The run can be terminated before 64 Triggers have been found by using the STOP key.

3-30. TRACE TRIGGERS End on DISABLE. In this mode the TRACE TRIGGERS measurement ends only when Trigger Disable is detected. The 1611A will display up to 64 Triggers that occurred immediately prior to detection of the Disable.

NOTE

Models 1611A with Serial Prefix 1723A and above (Opt Z80 installed) have this capability. If Trace Triggers end on Disable mode is desired in Models 1611A with Serial Prefix below 1723A, the old A8 board (01611-66508) must be changed to a modified A8 board (01611-66535).

To enter this mode: (1) Specify a BEFORE TRIG (PRETRIGR) of 63; (2) Specify a TRIGGER DISABLE; (3) Press TRACE TRIGS.

3-31. Trace Triggers and Trace Triggers End on Disable displays may be viewed in ABSOLUTE or MNEMONIC mode. In both modes the program or memory address of the Trigger is displayed in the ADRS column. In ABSOLUTE, the machine language op-code or data and the type of μP machine cycle (e.g., READ, OPCODE, WRITE) are displayed in the OPCODE/DATA column. In MNEMONIC, the assembly language mnemonic and 8 or 16 bit operand (if the operand exists) are displayed in the OPCODE/DATA column. If the operand is not captured by high-speed memory, then *** is shown in the appropriate line of OPCODE/DATA column. Hexadecimal or octal format can be selected and interchanged in both display modes.

3-32. Trace Triggers or Trace Triggers End on Disable measurements can be made in NORMAL or TRACE THEN HALT modes (selected by TEST MODE switch on Personality Panel A11). In NORMAL, the 1611A captures and displays Triggers while the μP system under test operates without interruption of program flow. In TRACE THEN HALT, the 1611A places the μP system under test in a Halt state when the data acquisition cycle is completed.

3-33. A TRACE TRIGGERS or TRACE TRIGGERS End on DISABLE measurement run is initiated each time TRACE TRIGS key is pressed. Repeated runs may be made with Continuous-run execution. Continuous execution is initiated by pressing TRACE TRIGS key approximately two seconds. The message CONTINUOUS will be displayed. Pressing the TRACE TRIGS key again restores regular operation. Continuous runs may be stopped by pressing STOP key or aborted by pressing any other key.

3-34. TRACE TRIGGERS SET-UP. Enter TRIGGER requirements. Trigger Enable and/or Disable requirements may be entered if desired. Ranges of address bus values which will be recognized as Triggers may also be entered with ADDRS BUS $\geqslant$ or $\leqslant$ keys. Triggering (including Enable and Disable) may be restricted to certain types of μP under test machine cycles with the TRIGGER QUALIFIER switches on Personality Panel A11. Press TRACE TRIGS key.

3-35. Display in TRACE TRIGGERS.

3-36. Before the first Trigger is detected two messages may be displayed. (1) WAITING FOR ENABLE flashes until the Enable specification (if entered) is detected. (2) WAITING FOR TRIGGER flashes until the Trigger specification is detected (after the Enable, if specified, has been detected).

3-37. WAITING FOR ENABLE and WAITING FOR TRIGGER can be alternating. This happens when both Enable and Disable are specified and no Trigger is found in the window. The Enable is found, no Trigger is found, the Disable is found, and the 1611A looks for another Enable.

3-38. During TRACE TRIGGERS End on DISABLE measurements, the message TRIGR OCCUR = 0 flashes (instead of WAITING FOR TRIGGER) until the first Trigger is detected.

3-39. After the first Trigger is detected, but before the TRACE TRIGGERS measurement is complete, the message TRIGR OCCUR = may appear. This shows how many Triggers are detected from the first Trigger until high-speed memory is full (64 Triggers Stored).

3-40. In Trace Triggers End on Disable measurements, the message TRIGR OCCUR = >64 can appear for two reasons: (1) When 64 Triggers are detected before the Disable is detected; (2) The 1611A does not contain the TRACE TRIGGERS End on DISABLE modification (1611A with Serial Numbers Prefix below 1723A).

3-41. Any data shown below the dashed line will not change until the measurement is complete or until data acquisition is stopped by the STOP key. When a measurement is completed, the message TRACE TRIGGERS appears. Triggers are shown in the data display (figure 3-9). The message LINE 0 also appears. The DISPLAY ROLL keys may be used to move the 16-line display window through the 64 lines (0 to 63) stored in high-speed memory. The line message will vary from 0 to 48. The LINE number shown is the number of the top line in the 16-line display (48 + 15 = 63). TRACE TRIGGERS End on DISABLE measurements can result in partial displays. This is because less than 16 Triggers were detected before Disable.

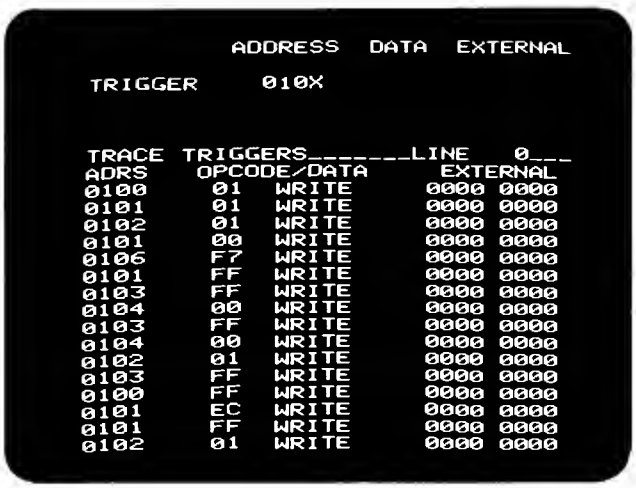


Figure 3-9. Trace Trigs Display

3-42. If an incomplete TRACE TRIGGERS or TRACE TRIGGERS End on DISABLE measurement is stopped by the STOP key, then all data acquired by the high-speed memory during the measurement will be displayed (memory dump). If the memory has no new data, then the data display section will be blank. The message STOPPED is shown.

3-43. When a TRACE TRIGGERS or TRACE TRIGGERS End on DISABLE measurement is incomplete and any key other than an EXECUTE key is pressed, the measurement is aborted. The display remains as it was before the measurement. Any attempt to change the display with DISPLAY Group Keys will result in the message RUN ABORTED, NO DISPLAY CHANGE.

3-44. COUNT TRIGGERS MEASUREMENT EXECUTION.

3-45. COUNT TRIGGERS. In this mode the 1611A counts Triggers detected between (and including) the Trigger Enable and Trigger Disable words. Count Triggers measurements can be performed in two ways: (1) A regular measurement run is executed each time COUNT TRIGS key is pressed; (2) Repeated COUNT TRIGGERS runs are made with Continuous-run execution. COUNT TRIGGERS measurements are made with TEST MODE switch on Personality Panel A11 in the NORMAL position.

3-46. A COUNT TRIGGERS measurement run is initiated each time COUNT TRIGS key is pressed. Repeated COUNT TRIGGERS runs may be made with Continuous-run execution (initiated by pressing COUNT TRIGS key approximately two seconds). The message CONTINUOUS will be displayed. Pressing COUNT TRIGS keys again restores regular operation. Continuous runs may be stopped by pressing STOP key or aborted by pressing any other key.

3-47. COUNT TRIGGERS SET-UP. Enter Trigger ENABLE, TRIGGER, and Trigger DISABLE requirements. Ranges of address bus values which will be recognized as triggers may also be entered with ADDRS BUS $\geqslant$ or $\leqslant$ keys. Triggering (including Enable and Disable) may be restricted to certain types of μP under test machine cycles with the TRIGGER QUALIFIER switches on Personality Panel A11. Press COUNT TRIGS Key.

3-48. Display in COUNT TRIGGERS.

3-49. Before Enable is detected, the message WAITING FOR ENABLE flashes. The bottom line of the data display will show COUNT = 0 TRIGGERS. This line shows the incomplete result of a count in progress. After the Enable is detected, but before the DISABLE is detected, the message COUNTING may flash and the bottom line COUNT = shows how many triggers have been detected. If the cumulative count exceeds 2^{24} -1 (approximately 16.78 x 10^6) Triggers, then the message COUNTER OVERFLOW flashes. This means that the Disable was not detected before the counter limit was exceeded.

3-50. When the Disable is detected the measurement is completed (figure 3-10). The bottom line of the data display COUNT = disappears. The top line of the data display COUNT = shows how many Triggers were detected between (and including) the Enable and Disable. MAX = and MIN = show the same number of Triggers detected as COUNT=. This is because both the maximum and minimum results of the first COUNT TRIGS run are the same as the completed measurement result.

3-51. In COUNT TRIGGERS Continuous-run execution, the bottom line COUNT = will often be flashing. This is due to updating of the incomplete result of a count in progress. The top line COUNT = shows the result of the last measurement completed. MAX = shows the maximum number of Triggers detected by any of the repeated executions of Count Triggers. MIN = shows the minimum number of Triggers detected by any of the repeated executions of Count Triggers.

3-52. Any COUNT TRIGGERS measurement in progress may be stopped with the STOP key or aborted with any other key. When the STOP key is pressed while a run is in progress, the message STOPPED appears.

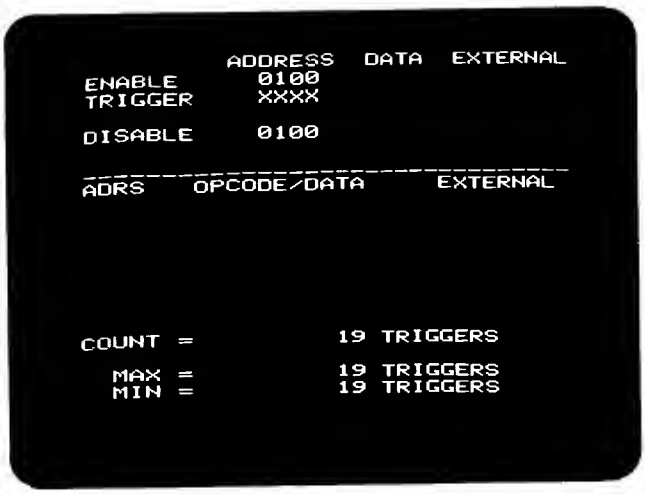


Figure 3-10. Count Triggers Display

3-53. TIME INTERVAL MEASUREMENT EXECUTION.

3-54. TIME INTERVAL. This mode produces a readout of elapsed time between the occurrence of two states defined by Trigger Enable and Trigger Disable. The timing measurement is made using an internal 1 MHz reference oscillator. Accuracy is within 0.1% ±1μs. Verifying the execution time of wait loops is one application of the time interval feature. It is also useful for measuring time required for the execution of a subroutine when a critical timing interface is involved with the system hardware or an external device. Time Interval measurements can be performed in two ways: (1) A regular measurement run is executed each time TIME INTVL key is pressed; (2) Repeated TIME INTERVAL runs are made with Continuous-run execution. Time Interval measurements are made with TEST MODE switch on Personality Panel A11 in the NORMAL position.

3-55. A TIME INTERVAL measurement run is initiated each time TIME INTVL key is pressed. Repeated TIME INTERVAL runs may be made with Continuous-run execution. This is initiated by pressing TIME INTVL key approximately two seconds. The message CONTINUOUS will be displayed. Pressing TIME INTVL key again restores regular operation. Continuous runs may be stopped with STOP key or aborted by pressing any other key.

3-56. TIME INTERVAL SET-UP. Enter Trigger ENABLE and Trigger DISABLE requirements. NO TRIGGER entry is required. The Enable and Disable may both be restricted to certain types of μP under test machine cycles with the TRIGGER QUALIFIER switches on Personality Panel A11. Press TIME INTVL key.

3-57. Display in TIME INTERVAL.

3-58. Before the Enable is detected, the message WAITING FOR ENABLE flashes. The bottom line of the data display will show TIME = 0 MICROSECONDS. This line shows the incomplete result of a count in progress. After the Enable is detected, but before the DISABLE is detected, the message COUNTING may flash and the bottom line TIME = shows the elapsed time in microseconds. If the cumulative count exceeds $2^{24}-1$ (approximately 16 seconds), then the message COUNTER OVERFLOW flashes. This means that the Disable was not detected before the counter limit was exceeded.

3-59. When the Disable is detected the measurement is completed (figure 3-11). The bottom line of the data display TIME = disappears. The top line of the data display TIME = shows elapsed time in microseconds between occurrence of the Enable and the Disable. MAX = and MIN = will show the same elapsed time as TIME =. This is because both maximum and minimum results of the first TIME INTVL run are the same as the completed measurement result.

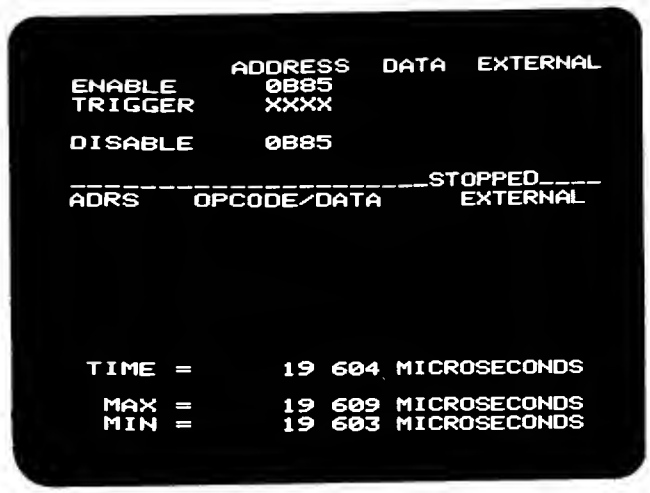


Figure 3-11. Time Interval Display

3-60. In TIME INTERVAL Continuous-run execution, the bottom line TIME = will often be flashing. This is due to updating of the incomplete result of a count in progress. The top line TIME = shows the result of the last measurement completed. MAX = shows maximum elapsed time of any repeated executions of Time Interval. MIN = shows minimum elapsed time of any repeated executions of Time Interval.

3-61. All TRIGGER field entries are ignored by the 1611A in Time Interval mode. Any Time Interval measurement in progress may be stopped with the STOP key or aborted with any other key.

3-62. OPERATOR'S CHECKS.

3-63. SELF-TEST. When power is applied to the 1611A, the internal microprocessor automatically performs an

internal self-test on the 1611A. A check sum is performed to verify contents of the ROM. Next, a test pattern is written to the RAM (to check for RAM ERROR), then read back and checked for accuracy. Also, some system hardware (most of the circuitry on A7 and A8 boards) is tested at this time. Upon completion of these tests, the message SELF-TEST COMPLETED is written on screen by the microprocessor to give a visual indication that the display circuitry and microprocessor are working properly. If a malfunction is detected, then the messages ERROR IN RAM, ERROR IN ROM, or ERROR IN HARDWARE may be displayed. These give quick indications of where to look when 1611A troubleshooting is necessary.

3-64. PROBE TEST. (Switch on probe must be in HOLD position during probe test.) Functional tests may be made on the 1611A without any external circuits by connecting the microprocessor probe plug into the Personality Panel Probe Test socket. Executing a trace generates a test display (see figure 3-12). Most system functions and controls may then be exercised on this pattern. In addition to generating a test pattern, the PROBE TEST feature permits checkout of Personality Panel indicators by cycling through NO CLOCK, HALT, WAIT, and INTERRUPT ACK lights at a 1-Hz rate. Check WAIT/HOLD BY 1611A light by setting TEST MODE switch to SINGLE STEP. Return TEST MODE switch to NORMAL.

3-65. STATUS MESSAGES. The following messages are displayed on the 1611A screen to provide an indication of 1611A operating status. (Messages may vary with different 1611A options.)

CONTINUOUS: Appears after an EXECUTE key has been held down approximately two seconds, which initiates continuous-run execution. Single run is restored by pressing the same key briefly. Continuous operation is stopped by STOP key, or aborted by pressing any other key.

COUNTER OVERFLOW: Appears in COUNT TRIGS or TIME INTERVAL mode when event counters overflow (Count exceeds 2^{24} -1).

COUNTING: Appears in COUNT TRIGS or TIME INTERVAL mode when 1611A is in the process of counting.

DELAYING: Displayed in TRACE mode from the time Trigger Occurrence specification has been met until the measurement is complete.

ERROR IN HARDWARE: Displayed when 1611A self-test has detected a malfunction in its internal hardware (on A7 or A8 boards).

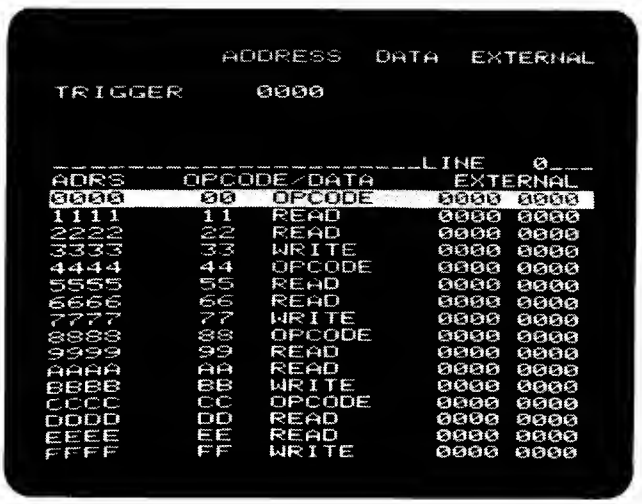
ERROR IN RAM/ROM: Appropriate message appears when self-test display comes on after turn-on if 1611A determines that random-access memory or read only memory is not functioning correctly.

ILLEGAL CHARACTER: Appears if the operator attempts to enter an unacceptable character into an open trace specification field. For example, attempting to enter an alpha character in the BEFORE TRIG field (decimal field) will generate this message.

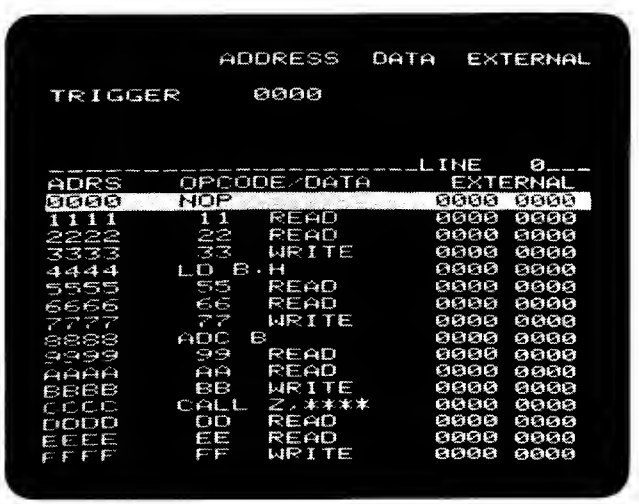
LINE 0 - 48: Indicates line number of top line in data display in TRACE and TRACE TRIGGERS modes. When LINE 48 is displayed, the next 15 lines on the display complete the 64 lines (0 to 63) stored in memory.

NO OPEN DATA FIELD: Displayed when the operator tries to enter a character from the ENTRY field without pressing appropriate key in the TRACE SPECIFICATION keyboard section to open a data field.

RUN ABORTED, NO DISPLAY CHANGE: Displayed for two conditions:



Absolute



Mnemonic

Figure 3-12. Probe Test Display

1. If a DISPLAY key is pressed when a TRACE or TRACE TRIGS run is in progress (WAITING FOR ENABLE, WAITING FOR TRIGGER, or the required number of TRIGR OCCUR has not been met).

2. If a DISPLAY key is pressed after a previous TRACE or TRACE TRIGS measurement run has been aborted by pressing any key other than an EXECUTE key while run is in progress.

SELF-TEST COMPLETED: Indicates satisfactory completion of self-test (unless an error message is also displayed).

SINGLE STEP: Displayed after TRACE is pressed in single-step mode.

SINGLE STEP, NO DISPLAY CHANGE: Displayed when an attempt is made to change the display by using DISPLAY keys after a trace has been executed in TRACE SINGLE STEP test mode.

SINGLE STEP, TRACE ONLY: Displayed when TEST MODE switch is set to SINGLE STEP and TRACE TRIGS, COUNT TRIGS, or TIME INTVL in the keyboard EXECUTE field is pressed. Only TRACE can be executed in SINGLE STEP test mode.

STOPPED: Displayed when STOP key is pressed, indicates a halt of any EXECUTE run in progress.

TRIGR OCCUR =: Displayed for three conditions:

1. During TRACE measurements, from first trigger recognition until number of triggers recognized equals the number selected by trigger occurrence specification.

2. During TRACE TRIGS measurements, from first trigger recognition until display memory is full (64 triggers stored).

3. During TRACE TRIGS End on Disable measurements, TRIGR OCCUR = 0 is displayed until first trigger is found, and TRIGR OCCUR= >64 is displayed if 64 triggers have been found without finding the Disable word, or if the 1611A does not contain the Trace Triggers End on Disable hardware modification (1611A with Serial Number Prefix below 1723A).

NOTE

If Trace Triggers End on Disable mode is desired, the old A8 board (01611-66508) may be changed to A8 board (01611-66535).

WAITING FORENABLE: Only displayed when a Trigger Enable has been specified and one of three conditions exists:

1. ENABLE specification has not been met.

2. System under test is running poorly or not at all.

3. This message will alternate with WAITING FOR TRIGGER if a trigger is not found between trigger ENABLE and DISABLE specifications, but the DISABLE is being found so the search for ENABLE is resumed.

WAITING FOR TRIGGER: Displayed for two conditions:

1. During TRACE and TRACE TRIGS measurements after Trigger ENABLE specification has been met, if an ENABLE has been specified, but before the first trigger has been detected.

2. Enable has not been specified and system under test is running poorly or not at all.

SECTION IV

PERFORMANCE TESTS

4-1. INTRODUCTION.

4-2. This section provides two types of performance tests: an Operation Verification and a Specification Verification. The Operation Verification provides approximately 90% assurance that the 1611A Option Z80 is functioning properly. The Specification Verification checks electrical parameters of the instrument using the specifications in table 1 as the performace standards. Unless the detailed specification Verification is required, it is recommended that only the Operation Verification be performed. All tests can be performed without access to the interior of the instrument.

4-3. PERFORMANCE TEST RECORD.

4-4. Performance Test results may be recorded in the Performance Test Record at the end of the procedures. The test record lists all tested specifications and their acceptable limits. The results recorded at incoming inspection can be used for comparison in periodic maintenance and troubleshooting and after repairs or adjustments.

4-5. OPERATION VERIFICATION.

4-6. To assure that the 1611A Option Z80 is operating properly without testing all the specifications listed in table 1, perform the following Operating Verification.

4-7. SELF-TEST

DESCRIPTION:

This test verifies proper operation of the ROM, display RAM, and some hardware circuits. If the ROM/RAM hardware test fails, the test will be repeated and a display indicating the failed circuit will be generated. When self test passes, a display is generated to indicate the circuit is operating properly.

PROCEDURE:

a. Set power LINE switch to on. Verify that CRT displays message SELF TEST COMPLETED.

4-8. MEMORY DISPLAY TEST.

DESCRIPTION:

This test verifies that the 1611A storage memory can be loaded and the information stored in memory can be viewed through a 16 line movable window. This test also verifies that information is being sensed correctly by the address and data lines.

PROCEDURE:

a. Connect μP probe A13 to front panel PROBE TEST socket.

b. Set 1611A front panel controls as follows:

ADRS-DATA BUS	HEXADECIMAL
I/O	OFF
WRITE	OFF
READ OP CODE	OFF
READ OP CODE	OFF
TEST MODE	NORMAL

c. Press TRACE key. Verify that a list is displayed.

d. Use ROLL keys to scroll through memory. Verify that LINE 0 through LINE 48 can be displayed.

NOTE

It may be necessary to use ABSOLUTE/MNEMONIC key to view all 64 lines of memory.

e. Press TRIGGER/ADDRESS BUS = key.

f. Enter 0000.

g. Press TRACE key. Verify the following display is shown in ABSOLUTE or MNEMONIC modes as below:

Figure 4-1. Absolute and Mnemonic Display

PERFORMANCE TESTS

4-9. STATUS MESSAGES FOR TRACE MODE TEST.

DESCRIPTION:
This test verifies that two messages are displayed before the first trigger condition is detected. WAITING FOR ENABLE flashes until the Enable specification (if entered) is detected. WAITING FOR TRIGGER flashes until the Trigger specification is detected.

PROCEDURE:
a. Press TRIGGER ENABLE/ADDRESS BUS = key.

b. Enter CDEF.

c. Press TRACE. Verify that WAITING FOR ENABLE message is flashing.

d. Press TRIGGER ENABLE/ADDRESS BUS = key.

e. Press DON'T CARE.

f. Press TRIGGER/ADDRESS BUS = key.

g. Enter 89AB.

h. Press TRACE key. Verify that WAITING FOR TRIGGER message is flashing.

4-10. TRIGGER ⩽, ⩾, TRIGGER OCCURENCES, DELAY AND TRACE TRIGGERS TEST.

DESCRIPTION:
This test verifies that the 1611A can recognize ⩽ or ⩾ trigger specification, count trigger occurrences, and count delay before the memory is loaded and a display is generated. This test also verifies that in TRACE TRIGGERS, only information matching Trigger conditions is stored in memory and displayed.

PROCEDURE:
a. Press ADRS BUS ⩾ key.

b. Enter 0000.

c. Press ADRS BUS ⩽ key.

d. Enter 1110.

e. Press TRIGGER OCCURRENCE key.

f. Enter 256.

g. Press AFTER TRIG key.

h. Enter 65472.

i. Press TRACE key. WAITING FOR TRIGGER message may flash briefly. Verify that DELAYING message flashes until trace is completed (LINE 0 displayed.)

j. Press TRACE TRIGGERS. Verify that every row of data display shows:

ADRS	OPCODE/DATA	EXTERNAL
0000	00 OPCODE	0000 0000

It may be necessary to use ABSOLUTE/MNEMONIC key to obtain this display.

PERFORMANCE TESTS

4-11. TRACE TRIGGERS END ON DISABLE TEST.

DESCRIPTION:
This test verifies that the 1611A can execute a TRACE TRIGGERS function which terminates only when a Triggers Disable condition is detected.

PROCEDURE:

a. Press and hold DON'T CARE key approximately three seconds until all TRACE SPECIFICATIONS are cleared.

b. Press TRIGGER/ADDRESS BUS = key.

c. Enter 0000.

d. Press BEFORE TRIG key.

e. Enter 63.

f. Press TRIGGER DISABLE/ADDRESS BUS = key.

g. Enter ABAB.

h. Press TRACE TRIGS.

i. Verify that TRIG OCCUR = 64 message flashes.

j. Press TRIGGER DISABLE/ADDRESS BUS = key.

k. Enter FFFF.

l. Press TRACE TRIGS key.

m. Verify that data display shows only one line as follows:

ADRS	OPCODE/DATA	EXTERNAL
0000	00 OPCODE	0000 0000

It may be necessary to use the ABSOLUTE/MNEMONIC key to obtain this result.

NOTE

If your 1611A serial number prefix is below 1723A, then TRIG OCCUR = 64 is displayed immediately to indicate that the 1611A does not have Trace Triggers End On Disable capability.

4-12. PRETRIGGER TEST.

DESCRIPTION:
This test verifies the ability to view a specified number of memory transactions that occur before a selected trigger word.

PROCEDURE:

a. Clear all TRACE SPECIFICATIONS entered on display by pressing the DON'T CARE key for approximately three seconds until all TRACE SPECIFICATIONS are cleared.

b. Press TRIGGER/ADDRESS BUS = key.

c. Enter AAAA.

d. Press BEFORE TRIGGER key.

e. Enter 4.

f. Press TRACE key. Verify that trigger word AAAA, in inverse video, is located on the 5th line of the display.

PERFORMANCE TESTS

4-13. COUNT TRIGGER TEST AND STOP TEST.

DESCRIPTION:
This test verifies that the 1611A can count Triggers detected between (and including) the Trigger Enable and Trigger Disable words. The test also verifies that operation is halted and STOPPED message is displayed when STOP key is pressed.

PROCEDURE:
a. Clear all TRACE SPECIFICATIONS entered on display by pressing the appropriate field selection keys and then pressing DON'T CARE key.

b. Press TRIGGER ENABLE/ADDRESS BUS = key.

c. Enter 0000.

d. Press TRIGGER DISABLE/ADDRESS BUS = key.

e. Enter FFFF.

f. Press TRIGGER/ADDRESS BUS = key.

g. Enter 4444.

h. Press and hold COUNT TRIGS key for approximately three seconds until CONTINUOUS message is displayed. Verify that COUNT =, MAX =, and MIN =, all display 1 TRIGGERS.

i. Press STOP key and verify that STOPPED message is displayed.

4-14. TIME INTERVAL TEST.

DESCRIPTION:
This test verifies that the 1611A can count the time interval occurring between states determined by Trigger Enable and Trigger Disable specifications. If no Trigger Disable condition is found, the COUNTER OVERFLOW, message occurs after approximately 16 seconds.

PROCEDURE:
a. Clear all TRACE SPECIFICATIONS entries on the display by pressing and holding the DON'T CARE key approximately three seconds until all TRACE SPECIFICATIONS are cleared. (NO OPEN DATA FIELD message will flash until the clear is complete.)

b. Press TRIGGER ENABLE/DATA BUS = key.

c. Enter 00.

d. Press TRIGGER DISABLE/DATA BUS = key.

e. Enter FF.

f. Press and hold TIME INTVL key for approximately three seconds until CONTINUOUS message is displayed. Verify that TIME =, MAX =, and MIN =, all display 30 microseconds (±1).

g. Press TRIGGER DISABLE/DATA BUS = key.

h. Enter AB.

i. Press TIME INTVL key. Verify that COUNTING, followed by COUNTER OVERFLOW messages are displayed (flashing).

PERFORMANCE TESTS

4-15. TRIGGER QUALIFIER SWITCH TEST.

DESCRIPTION:

This test verifies that the TRIGGER QUALIFIER switches can restrict triggering of the 1611A to certain types of machine cycles.

PROCEDURE:

a. Clear TRACE SPECIFICATIONS on the display by pressing and holding the DON'T CARE key for approximately three seconds until all TRACE SPECIFICATIONS are cleared.

b. Press TRACE key. Verify that list is displayed.

c. Set OCTAL/HEXADECIMAL switch to each position and verify that displayed data converts to selected base.

d. Set TRIGGER QUALIFIER I/O switch to I/O position.

e. Press TRACE key. Verify that WAITING FOR TRIGGER message is displayed.

f. Return I/O switch to OFF.

g. Set WRITE switch to WRITE position.

h. Press TRACE key. Verify that inverse video trigger displays WRITE in the OPCODE/DATA column.

i. Return WRITE switch to OFF position.

j. Set READ $\overline{\text{OP CODE}}$ switch to $\overline{\text{OP CODE}}$ position.

k. Press TRACE key. Verify that inverse video trigger displays READ or WRITE in the OPCODE/DATA column.

l. Return $\overline{\text{OP CODE}}$ switch to OFF.

m. Set READ OP CODE switch to OP CODE position.

n. Press TRACE key. Verify that inverse video trigger displays OPCODE read or write in the OPCODE/DATA column. It may be necessary to use ABSOLUTE/MNEMONIC key to obtain this display.

o. Return OP CODE switch to OFF.

p. Verify that NO CLOCK, BUS ACK, WAIT, HALT and RESET indicators light in sequence.

q. Set TEST MODE switch to TRACE SINGLE STEP. Verify that WAIT and WAIT by 1611A indicators are on.

r. Return TEST MODE switch to NORMAL.

s. Check TRIGGER QUALIFIER indicator by cycling I/O, WRITE, $\overline{\text{OPCODE}}$, and OP CODE switches on and off. All TRIGGER QUALIFIER switches must be OFF for TRIGGER QUALIFIER indicator to be extinguished.

END OF OPERATION VERIFICATION TESTS.

PERFORMANCE TESTS

4-16. SPECIFICATION VERIFICATION.

4-17. The following procedures test the electrical parameters of the 1611A Option Z80 using the specifications of table 1-1 as the performance standard. Threshold specifications are tested by applying the minimum voltage that the 1611A will recognize as a logic "1" and the maximum voltage that the 1611A will recognize as a logic "0". Setup time is the minimum time that data must be present at a 1611A probe input before it can be clocked into the 1611A. Hold time is the minimum time that data must be present at a 1611A probe input after it is clocked into the 1611A. When the minimum threshold, setup time, and hold time specifications are met, then known data that is clocked into the 1611A can be shown by the CRT (or front-panel indicators) to verify proper 1611A circuit operation.

4-18. TEST SIGNAL CONNECTIONS. No standard adapter is available for connecting test signals to microprocessor probe A13. Therefore, it is recommended that short lengths of small-gauge solid wire be inserted in the probe socket and that test signals be connected to these wires with a BNC-to-alligator clip adapter. The solid wires allow socket clamping action to secure a good connection between the signal source and the probe.

NOTE

Some tests will not give correct results if the wrong 1611A keys are accidentally pressed. If the 1611A does not give a correct indication, cycle LINE power switch off and on, and then repeat the test to verify that the incorrect indication was not caused by pressing the wrong key.

4-19. INITIAL SETUP.

a. Connect external probe A12 and μP probe A13 to their respective connectors on 1611A rear panel. Do not connect μP probe A13 to front-panel test socket.

b. Set 1611A front-panel controls as follows:

ADRS·DATA BUS ..... HEXADECIMAL
READ OP CODE ..... OFF
READ $\overline{\text{OP CODE}}$ ..... OFF
WRITE ..... OFF
I/O ..... OFF
TEST MODE ..... NORMAL

NOTE

Perform tests in the sequence given. Test equipment should not be disconnected unless specified in the procedure. Remove μP probe cable with 40-pin male connector from μP probe A13 during these tests. Do not specify an ENABLE. Specify TRIGGER = DON'T CARE.

NOTE

This performance test applies only to 10260A modules with A9 Board 01611-66561. Modules with A9 Board 01611-66523 or 01611-66540 will use different test waveforms as shown in Section VII.

PERFORMANCE TESTS

4-20. $\overline{RD}$, $\overline{WR}$, $\overline{IORQ}$ TEST.

SPECIFICATION:
Threshold; 2.0 volts minimum logic 1 (high); 0.7 volts maximum logic 0 (low).

DESCRIPTION:
This test verifies that a proper signal applied to the μP probe A13 $\overline{RD}$, $\overline{WR}$, or $\overline{IORQ}$ inputs will clock data into the 1611A for display on the CRT.

EQUIPMENT:
Pulse Generator (1) ..... HP 8012B
50 Ohm Feedthrough (1) 10100C
BNC to Alligator Clip Adapter (1) ..... HP P/N 8120-1291
Oscilloscope ..... HP 1740

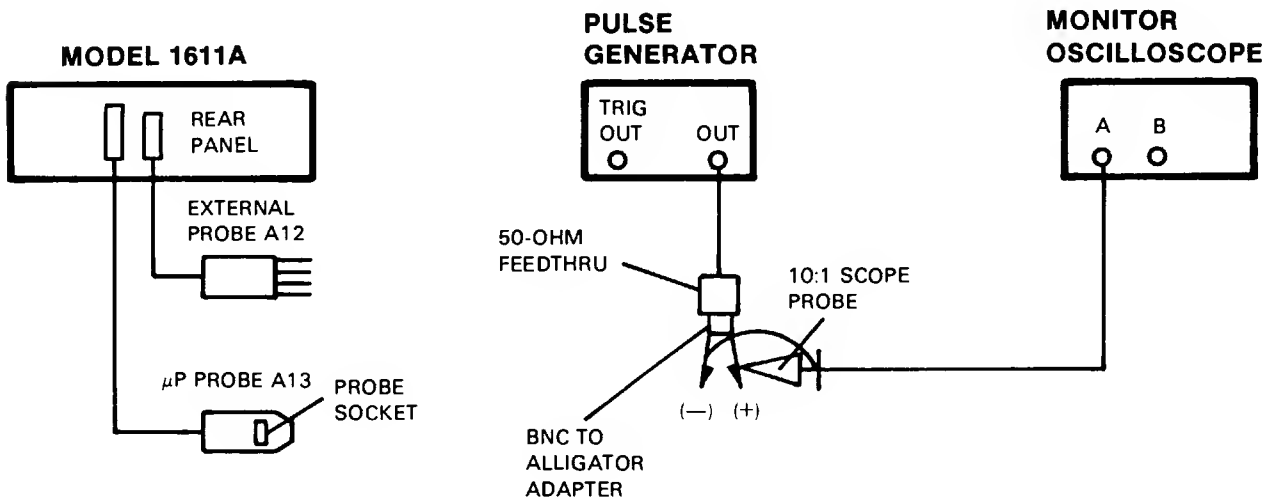


Figure 4-2. $\overline{RD}$, $\overline{WR}$, $\overline{IORQ}$ Test Setup.

PERFORMANCE TESTS

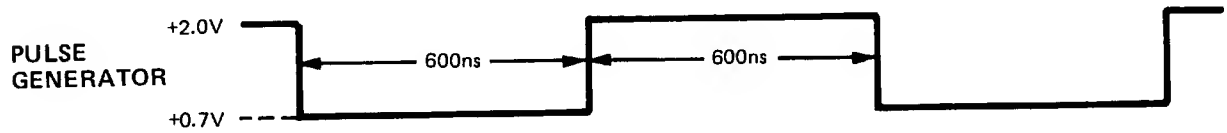


Figure 4-3. $\overline{RD}$, $\overline{WR}$, $\overline{IORQ}$ Test Waveform.

PROCEDURE:

a. Connect test equipment as shown in figure 4-2.

b. Adjust pulse generator for waveform shown in figure 4-3.

c. Connect pulse generator between pin 21 ($\overline{RD}$) and pin 29 (GND) of μP probe A13 test socket.

d. Press TRACE and verify that list is displayed.

NOTE

Since all Address and Data inputs are open (TTL HI), then all lines are latched HI. This results in $FFFF_{16}$ in ADRS column and FF_{16} in OPCODE/DATA column.

e. Remove pulse generator from pin 21 of μP probe A13.

f. Repeat steps c and d for $\overline{WR}$ and $\overline{IORQ}$ inputs and verify that data is clocked into the 1611A.

PERFORMANCE TESTS

4-21. DATA LINES TEST

SPECIFICATION:

Setup Time 40ns, Hold Time 0ns relative to rising edge of $\overline{RD}$, $\overline{WR}$, or $\overline{IORQ}$.
Threshold: 2 volts minimum logic 1 (high)
.7 volts maximum, logic 0 (low).

DESCRIPTION:

A LO pulse (logic "0") that satisfies minimum setup time, hold time, and threshold is applied to each Data input line and clocked into the 1611A by the signal $\overline{RD}$. The CRT display is then checked to verify proper operation of the Data line under test.

EQUIPMENT:

Pulse Generator (2) ..... HP 8012B
50 Ohm Feedthrough (2) ..... HP 10100C
BNC to Alligator Clip Adapter (2) ..... HP P/N 8120-1292
Oscillocope ..... HP 1740

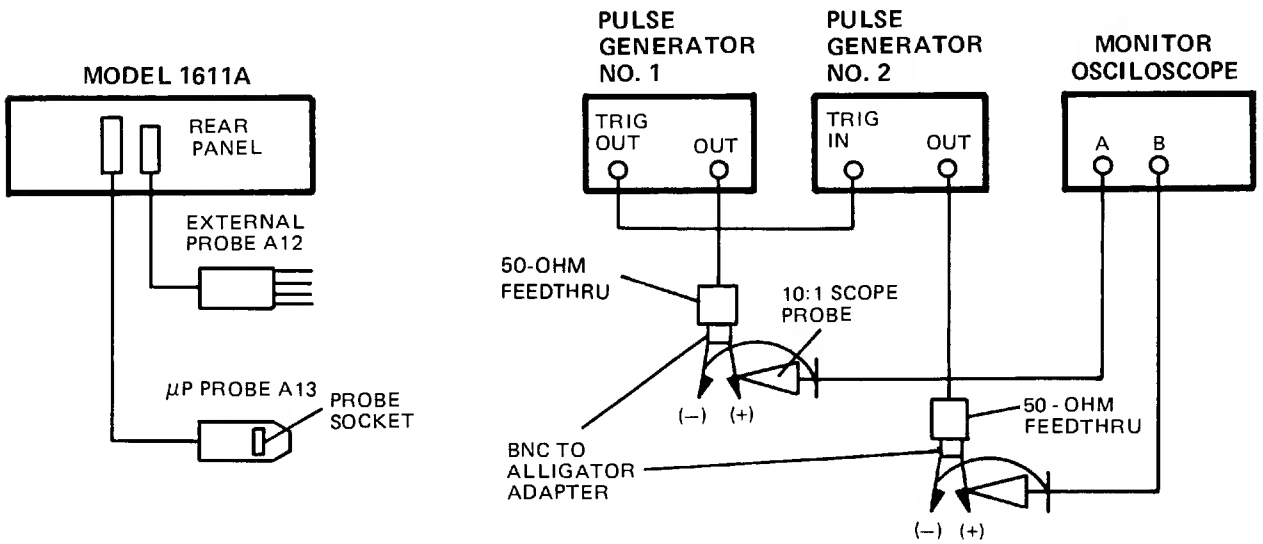


Figure 4-4. Data Test Setup

PROCEDURE:

a. Connect test equipment as shown in figure 4-4.

b. Connect pulse generator No. 1 between pin 21 ($\overline{RD}$) and pin 29 (GND).

c. Connect pulse generator No. 2 between 14 (D0) and pin 29 (GND).

d. Adjust pulse generators for waveforms shown in figure 4-5.

NOTE

For A9 Personality Board with Part No. 01611-66523, refer to figure 7-4.

e. Press TRACE key and verify that display fields contain information as follows:

PERFORMANCE TESTS

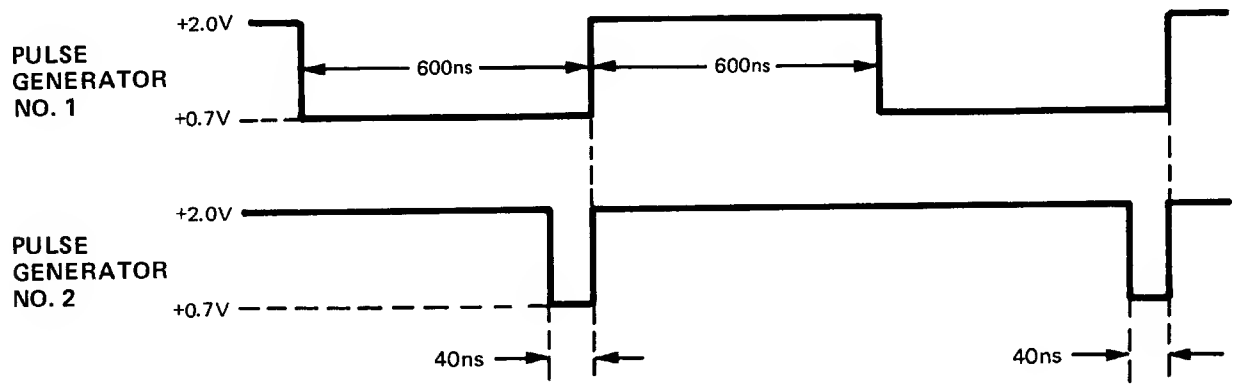


Figure 4-5. Data Lines Test Waveforms

ADRS	OPCODE/DATA	EXTERNAL
FFFF	FE INPUT	0000 0000

NOTE

Since all Address and Data inputs are open (TTL HI), then all lines are latched high unless pulsed low.

f. Disconnect pulse generator No. 2 from pin 14 of μP probe A13 test socket.

g. Repeat steps c through e for remaining Data lines and verify that OPCODE/DATA field agrees with table 4-1.

Table 4-1. OPCODE/DATA Field Display

Data Line	μP Probe A13 Socket Pin	OPCODE/DATA
D0	14	FE INPUT
D1	15	FD INPUT
D2	12	FB INPUT
D3	8	F7 INPUT
D4	7	EF INPUT
D5	9	DF INPUT
D6	10	BF INPUT
D7	13	7F INPUT

PERFORMANCE TESTS

4-22. ADDRESS LINES TEST

SPECIFICATION:

Setup Time 200ns minimum, Hold Time 0ns minimum relative to rising edge of $\overline{RD}$, $\overline{WR}$, or $\overline{IORQ}$.
Threshold: 2 volts minimum logic 1 (high)
.7 Volts maximum, logic 0 (low).

DESCRIPTION:

A LO pulse (logic "0") that satisfies minimum setup time, hold time, and threshold is applied to each Address input line and clocked into the 1611A by the signal $\overline{RD}$. The CRT display is then checked to verify proper operation of the Address line under test.

EQUIPMENT:

Pulse Generator (2)	HP 8012B
50 Ohm Feedthrough (2)	HP 10100C
BNC to Alligator Adapter (2)	HP P/N 8120-1292
Oscilloscope	HP 1740A

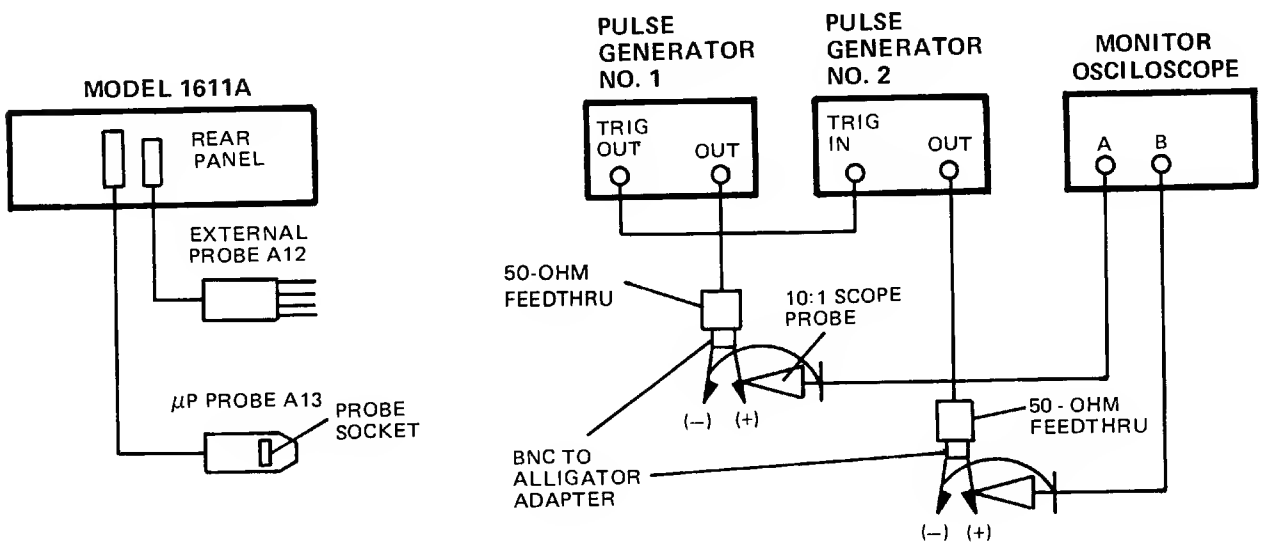


Figure 4-6. Address Lines Test Setup

PROCEDURE:

a. Connect test equipment as shown in figure 4-6.

b. Connect pulse generator No. 1 between pin 21 ($\overline{RD}$) and pin 29 (GND).

c. Connect pulse generator No. 2 between pin 30 (A0) and pin 29 (GND).

d. Adjust pulse generators for waveforms shown in figure 4-7.

NOTE

For A9 Personality Board with Part No. 01611-66523, refer to figure 7-5.

e. Press TRACE key and verify that display fields contain information as follows:

PERFORMANCE TESTS

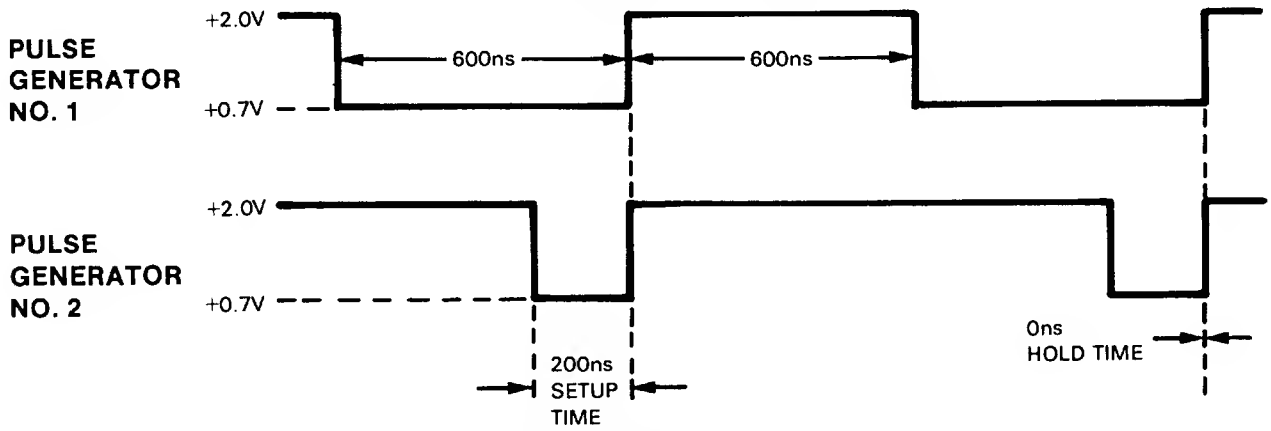


Figure 4-7. Address Lines Test Waveforms

ADRS	OPCODE/DATA	EXTERNAL
FFFE	FF INPUT	0000 0000

NOTE

Since all Address and Data inputs are open (TTL HI), then all lines are latched high unles pulsed low.

f. Disconnect pulse generator No. 2 from pin 30 of μP probe A13 test socket.

g. Repeat steps c through e for remaining Address lines and verify ADRS field agrees with table 4-2.

Table 4-2. ADRS Field Display

Address Line	μP Probe A13 Socket Pin	ADRS
A0	30	FFFE
A1	31	FFFD
A2	32	FFFB
A3	33	FFF7
A4	34	FFEF
A5	35	FFDF
A6	36	FFBF
A7	37	FF7F
A8	38	FEFF
A9	39	FDFF
A10	40	FBFF
A11	1	F7FF
A12	2	EFFF
A13	3	DFFF
A14	4	BFFF
A15	5	7FFF

PERFORMANCE TESTS

4-23. EXTERNAL PROBE INPUT TEST.

SPECIFICATION:

Setup Time 150 ns minimum; Hold Time 0ns minimum relative to rising edge of $\overline{RD}$, $\overline{WR}$, or $\overline{IORQ}$.
Threshold: 2.4V to 5.5V, logic 1 (high)
-0.8V to 0.8V, Logic 0 (low)

DESCRIPTION:

A HI pulse (logic "1") that satisfies minimum setup time, hold time, and threshold is applied to each External input line and clocked into the 1611A by the signal $\overline{RD}$. The CRT display is then checked to verify proper operation of the External input line under test.

EQUIPMENT:

Pulse Generator (2) ..... HP 8012B
50 Ohm Feedthrough (2) ..... HP 10100C
BNC to Alligator Adapter (2) ..... HP P/N 8120-1992
Oscilloscope ..... HP 1740A

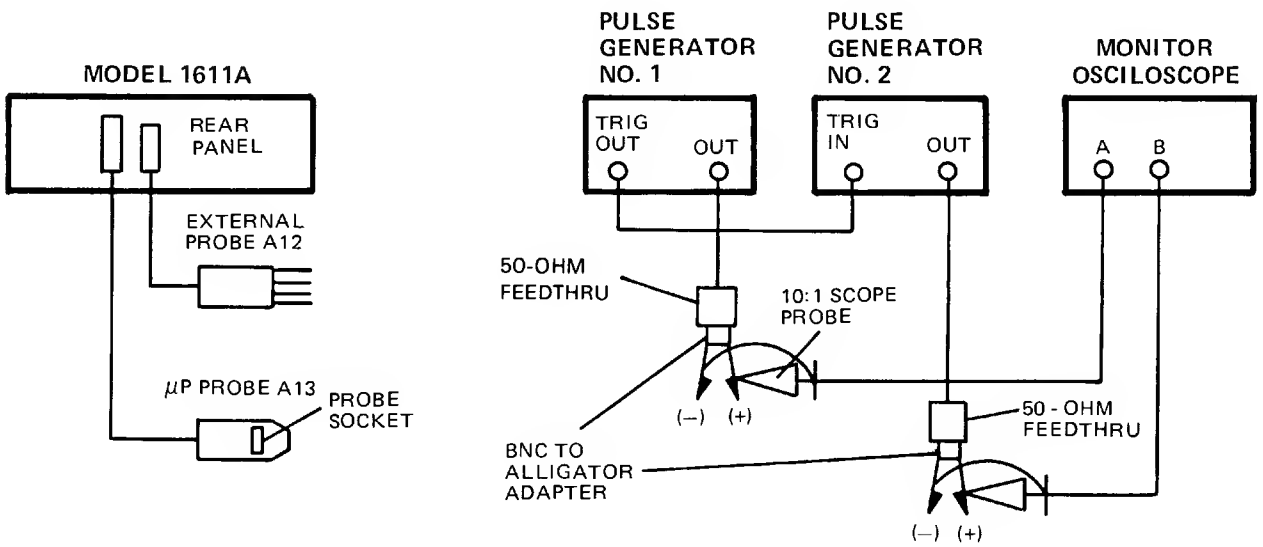


Figure 4-8. External Probe Input Test Setup

PROCEDURE:

a. Connect test equipment as shown in figure 4-8.

b. Connect pulse generator No. 1 between pin 21 ($\overline{RD}$) and pin 29 (GND).

c. Connect pulse generator No. 2 between input 0 and ground of external probe A12.

d. Adjust Pulse generators for waveforms shown in figure 4-9.

e. Press TRACE and verify that EXTERNAL field of input 0 matches that shown in table 4-3.

f. Disconnect pulse generator No. 2 from external input 0.

g. Repeat steps c and d for each remaining external input (1-7) and verify that EXTERNAL field in step c agrees with table 4-3 for each external line.

PERFORMANCE TESTS

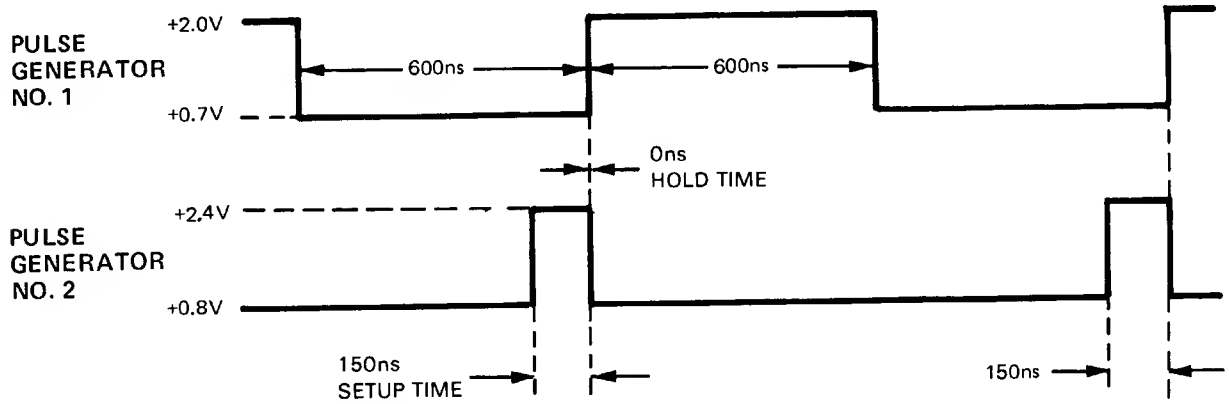


Figure 4-9. External Probe A12 Test Waveforms

Table 4-3. EXTERNAL Field Display

External Input	EXTERNAL
0	0000 0001
1	0000 0010
2	0000 0100
3	0000 1000
4	0001 0000
5	0010 0000
6	0100 0000
7	1000 0000

PERFORMANCE TESTS

4-24. REAR-PANEL OUTPUTS.

These tests verify that the 1611A produces proper Rear Panel Outputs.

PROCEDURE:

a. Plug 40-pin male connector from microprocessor probe cable into 1611A front-panel PROBE TEST socket. (Reconnect probe cable to probe if disconnected.)

b. Connect TRIGGER OUTPUT to oscilloscope as shown in figure 4-10 and verify that TRIGGER OUTPUT pulses have maximum amplitude greater than +2.0V and minimum amplitude less than +0.4 V.

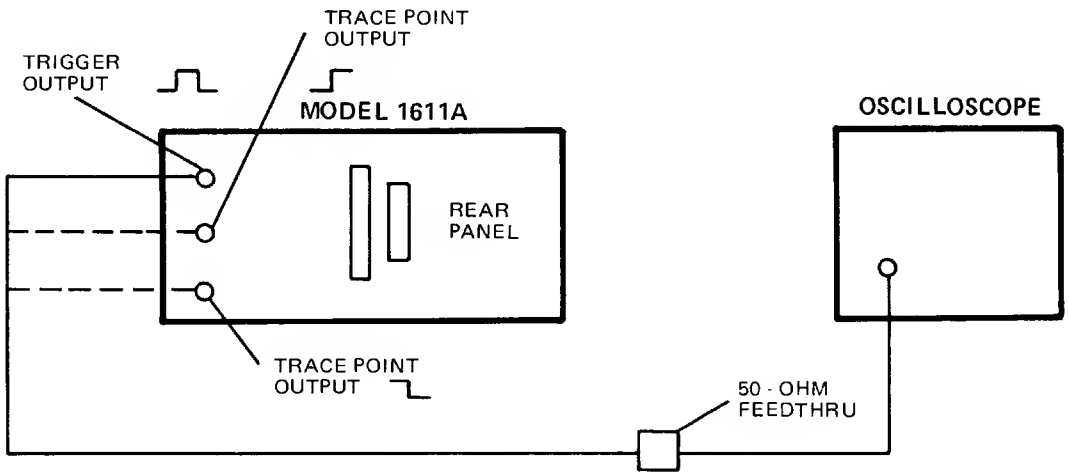


Figure 4-10. Rear-panel Outputs Test Setup

4-25. TRACE POINT ⌐ / ¬ OUTPUTS.

a. Connect TRACE POINT ⌐ output from 1611A rear panel to oscilloscope.

b. While holding TRACE down, verify presence of pulses on TRACE POINT ⌐ output with maximum amplitude greater than +2.0 V and minimum amplitude less than +0.4 V.

c. Disconnect TRACE POINT ⌐ output from oscilloscope and connect TRACE POINT ¬ output to oscilloscope.

d. While holding TRACE down, verify presence of pulses on TRACE POINT ¬ output with maximum amplitude greater than +2.0 V and minimum amplitude less than +0.4 V.

PERFORMANCE TEST RECORD

HEWLETT-PACKARD

MODEL 1611A Option Z80

LOGIC ANALYZER

Tested by _____

Serial No. _____ **Date** _____

Paragraph Number	Test	Specification	Passed	Failed
4-20	$\overline{RD}$, $\overline{WR}$, $\overline{IORQ}$	$0 \leq +0.7$ V, $1 \geq +2.0$ V, 1.2 μs cycle (symmetrical)	_____	_____
4-21	Data Lines D_0 - D_7	$0 \leq +0.7$ V, $1 \geq +2.0$ V Setup $\geq$ 40 ns Hold $\geq$ 0 ns	_____	_____
4-22	Address Lines A_0 - A_{15}	$0 \leq +0.7$ V, $1 \geq +2.0$ V, Setup $\geq$ 200 ns Hold $\geq$ 0 ns	_____	_____
4-23	External Inputs 0 - 7	$0 \leq +0.8$ V, $1 \geq +2.4$V Setup $\geq$ 150 ns Hold $\geq$ 0 ns	_____	_____
4-24	Trigger Output	$0 \leq +0.4$ V, $1 \geq 2.0$ V into 50Ω	_____	_____
4-26	Trace Point Ouputs	$0 \leq +0.4$ V, $1 \geq 2.0$ V into 50 Ω	_____	_____

SECTION V

ADJUSTMENTS

There are no adjustments on the Model 10260A/1611A Option Z80.

SECTION VI

REPLACEABLE PARTS

6-1. INTRODUCTION.

6-2. Table 6-1 lists all replaceable parts for the Model 10260A/1611A Option Z80. Replaceable parts are listed in reference designator order.

Table 6-1. Replaceable Parts

Ref Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
A9	01611-66561		8OARD ASSEM8LY, OPTION Z80 PERSONALITY	28480	01611-66561
A10	01611-66524		8OARD ASSEM8LY, OPTION Z80 ROM	28480	01611-66524
A11	01611-68704		ASSEM8LY, OPTION Z80 PERSONALITY PANEL	28480	01611-68704
A13	01611-62105		ASSEM8LY Z80/MICROPROCESSOR PRO8E	28480	01611-62105
MP1	1540-0325	1	CASE, CRVG HANDLE	28480	1540-0325
A9	01611-66561	1	8OARD ASSEM8LY, OPTION Z80 PERSONALITY	28480	01611-66561
A9C1 THRU A9C19	0160-0939	19	CAPACITOR-FXD 430PF	28480	0160-0939
A9C20 THRU A9C24			NOT USED ON 01611-66561 8OARD		
A9C25	0140-0204	1	CAPACITOR-FXD 47PF +-5% 500VDC	28480	0140-0204
A9C26	0160-0159	1	CAPACITOR-FXD 6800PF +-10% 200 VDC	28480	0160-0159
A9C27 THRU A9C36	0160-2055	10	CAPACITOR-FXD .01UF +80-20% 100V0C CER	28480	0160-2055
A9C37	0180-0228	1	CAPACITOR-FXD 22UF +-10% 15VDC TA	56289	150D226X901582
A9J1	1251-3024	1	CONNECTOR-26 PIN MALE RECTANGULAR	04726	3429-2002
A9R1 THRU A9R16	0757-0410	19	RESISTOR-FXD 301 1% .125W F TC=0+-100	28480	0757-0410
A9R17	0757-0438	1	RESISTOR-FXD 5.11K 1% .125W F TC=0+-100	28480	0757-0438
A9R18	0757-0457	1	RESISTOR-FXD 47 5K 1% .125W F TC=0+-100	28480	0757-0457
A9R19 THRU A9R21	0757-0410		RESISTOR-FXD 301 1% .125W F TC=0+-100	28480	0757-0410
A9TP1 THRU A9TP5	0360-0535	5	TEST POINT-TERM PC8	28480	0360-0535
A9U1	1820-1204	2	IC SN74LS20N TTL LS DUAL 4 NAND	01295	SN74LS20N
A9U2	1820-1217	1	IC SN74LS151N TTL LS DATA SEL/MUX	01295	SN74LS151N
A9U3	1810-0283	1	NETWORK-RES 16-PIN-DIP 270	01607	316B271
A9U4	1820-0579	1	IC SN74123N TTL DUAL MONO MV	01295	SN74123N
A9U5	1820-1307	1	IC SN74S132N TTL S OUAD 2 SCHMITT NAND	01295	SN74S132N
A9U6	1820-1201	2	IC SN74LS08N TTL LS QUAD 2 AND	01295	SN74LS08N
A9U7 THRU A9U10	1820-1196	5	IC SN74LS174N TTL LS HEX D F-F	01295	SN74LS174N
A9U11	1820-1195	1	IC SN74LS175N TTL LS QUAD D F-F	01295	SN74LS175N
A9U12	1820-1202	2	IC SN74LS10N TTL LS TRIPLE 3 NAND	01295	SN74LS10N
A9U13	1820-1112	3	IC SN74LS74N TTL LS DUAL D F-F	01295	SN74LS74N
A9U14	1820-1425	1	IC SN74LS132N TTL LS OUAD 2 SCHMITT NAND	01295	SN74LS132N
A9U15	1820-0685	1	IC SN74S10N TTL S TRIPLE 3 NAND	01295	SN74S10N
A9U16	1820-1416	1	IC SN74LS14N TTL LS HEX SCHMITT INVERTER	01295	SN74LS14N
A9U17	1820-1112		IC SN74LS74N TTL LS DUAL D F-F	01295	SN74LS74N
A9U18	1820-0099	1	IC SN7493N TTL 8INARY COUNTER	01295	SN7493N
A9U19	1820-1144	1	IC SN74LS02N TTL LS QUAD 2 NOR	01295	SN74LS02N
A9U20	1820-1197	1	IC SN74LS00N TTL LS QUAD 2 NAND	01295	SN74LS00N
A9U21	1820-1201		IC SN74LS08N TTL LS QUAD 2 AND	01295	SN74LS08N
A9U22	1820-1202		IC SN74LS10N TTL LS TRIPLE 3 NAND	01295	SN74LS10N
A9U23	1820-1199	1	IC SN74LS04N TTL LS HEX INVERTER	01295	SN74LS04N
A9U24	1820-1112		IC SN74LS74N TTL LS DUAL D F-F	01295	SN74LS74N
A9U25	1820-1282	1	IC SN74LS109N TTL LS DUAL J-K F-F	01295	SN74LS109N
A9U26	1820-1191	2	IC SN74S175N TTL S QUAD D F-F	01295	SN74S175N
A9U27	1820-1191		IC SN74S175N TTL S QUAD D F-F	01295	SN74S175N
A9U28	1820-1204		IC SN74LS20N TTL LS DUAL 4 NAND	01295	SN74LS20N
A9U29	1820-1196		IC SN74LS174N TTL LS HEX D F-F	01295	SN74LS174N
A9U30	1820-0495	1	IC SN74154N TTL DEC/DEMUX	01295	SN74154N
A9U31 THRU A9U34	1820-1139	4	IC TTL HEX INVERTER	28480	1820-1139
A10	D1611-66568	1	8OARD ASSEM8LY, OPTION Z80 ROM	28480	01611-86568
A10C1	180-0228	1	CAPACITOR-FXD 22UF +-10% 15VDC TA	56289	150D226X901582
A10C2	0160-3443	1	CAPACITOR-FXD .1UF +80-20% 50 VDC CER	02813	CY20C104Z2
A10C3 THRU A10C6	0160-2055	4	CAPACITOR-FXD .01UF +80-20% 100 VDC CER	28480	0160-2055
A10R1	0757-0904	1	RESISTOR FXD 150 2% 125W	28480	0757-0904
A10U1	1820-1195	2	IC SN74LS175N TTL LS QUAD F-F	01295	SN74LS175N
A10U2	1820-1195		IC SN74LS175N TTL QUAD F-F	01295	SN74LS175N

Table 6-1. Replaceable Parts (Cont'd)

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
A10U3	1820-1208	1	IC SN74LS32N TTL LS QUAD 2 OR	01295	SN74LS32N
A10U4	1820-1917	1	IC SN74LS240N TTL LS 3-STATE OCTAL LN DRVR/RCVR	01295	SN74LS240N
A10U5			DELETED		
A10U6			DELETED		
A1DU7	1816-1106	1	IC 82S181 DE87 ROM	28480	1816-1106
A10U8	1816-1107	1	IC B2S181 DE88 ROM	28480	1816-1107
A10U9	1818-0707	1	IC 82S181 DE89 ROM	28480	1818-0707
A10U10	1818-0711	1	IC 82S181 SL=0G1 ROM	28480	1818-0711
A10U11	1820-1216	1	IC SN74LS13BN TTL LS DEC/MUX	01295	SN74LS138N
A10U12	1810-0055	1	NETWORK-RES 9-PIN-SIP 15-PIN-SPCG 10K	28480	1810-0055
A10XU5 THRU A10XU10	1200-0622	6	SOCKET-IC 24-PIN-DIP	28480	1200-0622
A11	01611-88712	1	ASSEMBLY, OPTION Z80 PERSONALITY PANEL	28480	01611-68712
A11H1	2200-0103	4	SCREW-MACH 4-40 .250-IN-LG PAN-HD-POZI	28480	2200-0103
A11MP1	D1611-00211	1	PANEL, A18 PERSONALITY	28480	01611-00211
A11MP2	5040-0565	1	BEZEL CONNECTOR	28480	5040-0585
A11A1	01611-66573	1	PANEL PERSONALITY Z80	28480	01611-66573
A11A1C1	0160-3508	2	CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3508
A11A1C2	0160-3508		CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	016D-3508
A11A1DS1 THRU A11A1DS6	1990-0486	6	LED-VISIBLE RED LUM-INT=1MCD IF=20MA-MAX	28480	1990-0486
A11A1DS7	1990-0487	1	LED-VISIBLE YELLOW LUM-INT=1MCD IF=20MA-MAX	28480	1990-0487
A11A1J1	1200-0623	1	CONNECTOR-40-PIN FEM ZIF	28480	1200-0623
A11A1R1 THRU A11A1R7	0684-2711	7	RESISTOR-FXD 270 10% .250W FC TC=-400/+600	28480	0684-2711
A11A1R8	0684-1021	1	RESISTOR-FXD 1K 10% .250 W FC TC=400/+600	28480	0684-1021
A11A1R9	0757-0420	2	RESISTOR-FXD 750 1% .125W F TC 0±100	07716	CEA-993
A11A1R10	0757-0420	1	RESISTOR-FXD 750 1% .125W F TC 0±100	D7716	CEA-993
A11A1S1	3101-2118	4	SWITCH-TGL SU8MIN SPDT NS 2A 250VAC	28480	3101-2118
A11A1S2 THRU A11A1S5	31D1-2214		SWITCH-TGL SU8MIN SPDT NS 2A 250VAC	28480	3101-2214
A11A1S6	3101-2119	1	SWITCH-TGL SU8MIN DPDT NS 2A 250VAC		3101-2119
A13	01611-62105	1	ASSEM8LY, Z80/MICROPROCESSOR PRO8E	2848D	01611-62105
A13H2	D624-0309	2	SCREW-TPG 6-19 .375-IN-LG HEX-HD STL	28480	0624-0309
A13MP1	5040-8126	1	PRO8E POD, BOTTOM	28480	5040-8126
A13MP2	5040-8124	1	PRO8E POD, TOP	28480	5040-8124
A13MP3	7120-6461	1	LABEL, Z80 PROBE	28480	7120-6461
A13MP4	1540-0440	1	CASE, VINYL	28480	1540-0440
A13W1	01611-61610	1	CABLE ASSEMBLY, DIP-LONG	28480	01611-6161D
A13W1	01611-61612	1	CABLE ASSEM8LY, DIP-SHORT (NOT SUPPLIED WITH A13 ORDER SEPARATELY)	28480	01611-61612
A13W2	01611-61623	1	CABLE ASSEM8LY-MICROPROCESSOR PRO8E	28480	01611-61623
A13W2H1	2200-0111	2	SCREW-MACH 4-40 5-IN-LG PAN-HD-POZI	28480	2200-0111
A13W2H2	3050-0235	2	WASHER-FL MTCL NO.-4 .117-IN-ID	2848D	3050-0235
A13W2H3	2190-0019	2	WASHER-LK HLCL NO.-4 .115-IN-ID	2848D	2190-0019
A13W2H4	2260-0002	2	NUT-HEX-D8L-CHAM 4-40-THD .062-THK	28480	2260-0002
A13W2MP1	01611-81201	1	CLAMP, CABLE	28480	01611-61201
A13A1	01811-66541	1	8OARD ASSEM8LY, PROBE	28480	01611-66541
A13A1C1	0180-2228	1	CAPACITOR-FXD 22UF +-10% 15VDC TA	56289	150D226X901582
A13A1C2	0160-3508	1	CAPACITOR-FXD 1UF +80-20% 50VDC CER	2848D	0160-3508
A13A1C3 THRU A13A1C5	0160-3451	3	CAPACITOR-FXD .01UF	28480	0160-3451
A13A1C6	0160-3446	1	CAPACITOR-FXD 220PF±10% 1KVDC CER	28480	0160-3446
A13A1J1	1200-0623	1	CONNECTOR-40-PIN FEM ZIF	28480	1200-0623
A13A1P1	1251-3782	1	CONNECTOR-40-PIN MALE RECTANGULAR	76381	3432-1002
A13A1R1	0757-0409	2	RESISTOR-FXD 274 1% .125W F TC=0+-100	28480	0757-0409
A13A1R2	0757-0409		RESISTOR-FXD 274 1% .125W F TC=0+-100	28480	0757-0409
A13A1U1	1820-2160	5	IC SN74LS244N TTL LS OCTAL BUFF/LN DRV/LN RCVR	01295	1820-2160
A13A1U2	1810-0283	4	NETWORK-RES 16-PIN-DIP 270	01607	316B271
A13A1U3	1820-2160		IC SS74LS244N TTL LS OCTAL BUFF/LN DRV/LN RCVR	01295	SN74LS244N
A13A1U4	1810-0283		NETWORK-RES 16-PIN-DIP 270	01607	3168271
A13A1U5	1820-2160		IC SN74LS244N TTL LS OCTAL BUFF/LN DRV/LN RCVR	01295	SN74LS244N
A13A1U6	1820-1200	1	IC SN74LSD5N TTL LS HEX INV OC	01295	SN74LS05N
A13A1U7	1820-2160		IC SN 74LS244N TTL LS OCTAL 8UFF/LN DRV/LN RCVR	01295	SN74LS244N
A13A1U8	1810-0283		NETWORK-RES 16-PIN-DIP 270	01607	3168271
A13A1U9	1820-2160		IC SN74LS244N TTL LS OCTAL 8UFF/LN DRV/LN RCVR	01295	SN74LS244N
A13A1U10	1810-0283		NETWORK-RES 16-PIN-DIP 270	01607	316B271

SECTION VII

MANUAL CHANGES

7-1. INTRODUCTION.

7-2. This section contains information for adapting this manual to options for which the content does not apply directly.

7-3. MANUAL CHANGES.

7-4. To adapt this manual to your option, refer to table 7-1 and make all of the manual changes listed opposite your option serial number or PC Board number. Perform these changes in the sequence listed.

7-5. If your option serial number is not listed on the title page of this manual or in table 7-1 below, it may be documented in a yellow MANUAL CHANGES supplement.

Table 7-1. Manual Changes

Serial Prefix	Make Change
Z80 Opt with A13A1 Probe Board 01611-66526 installed.	1
Z80 Opt with A9 Personality Board 01611-66523 installed.	2,4
1817A	3
Z80 Opt with A9 Personality Boards 01611-66523 or 01611-66540 installed	5
1830A	6

7-6. MANUAL CHANGE INSTRUCTIONS.

CHANGE 1

Table 6-1:
A13A1U1, U3, U5, U7, U9: Change to HP Part No. 1820-1918, IC SN74LS241N, Mfr. Code 01295, Mfr. Part No. SN74LS241N.
Figure 8-1,
Service Sheet 1: Replace with figure 7-1.

CHANGE 2

Table 6-1:
Add: A9C1-24, HP Part No. 0140-0216, CAPACITOR-FXD 120PF 300VDC.
A9R1-16, HP Part No. 0757-0408, RESISTOR-FXD .12MF 243 1.
Delete: A9U30-34.
A9U23: Change to HP Part No. 1820-0683, IC SN74S04N, Mfr Code 01295, Mfr Part No. SN74S04N.
A9U22: Change to HP Part No. 1820-0685, IC SN74S10N, Mfr Code 01295, Mfr. Part No. SN74S10N.
A9U29: Change to HP Part No. 1820-0686, IC SN74S11N, Mfr Code 01295, Mfr. Part No. SN74S11N.
A9U28: Change to HP Part No. 1820-0688, IC SN74S20N, Mfr Code 01295, Mfr Part No. SN74S20N.
A9U26-27: Change to HP Part No. 1820-1196, IC SN74LS174N, Mfr Code 01295, Mfr. Part No. SN74LS174N.
A9U21: Change to HP Part No. 1820-1367, IC SN74S08N, Mfr Code 01295, Mfr Part No. SN74S08N.
Add: A9L1-24, HP Part No. 9100-1616, COIL-FXD, .50UH 160MC.
Figure 8-2,
Service Sheets 2A-B: Replace with figure 7-2 (4 sheets).

CHANGE 3

Table 6-1:
Delete: A9C1-19, A9R1-16, A9L1-38.
A9U29: Change to HP Part No. 1820-1195, IC SN74LS175N, Mfr Code 01295, Mfr Part No. SN74LS175N.
Figure 8-2,
Service Sheets 2A-B: Replace with figure 7-3 (3 sheets).

CHANGE 4

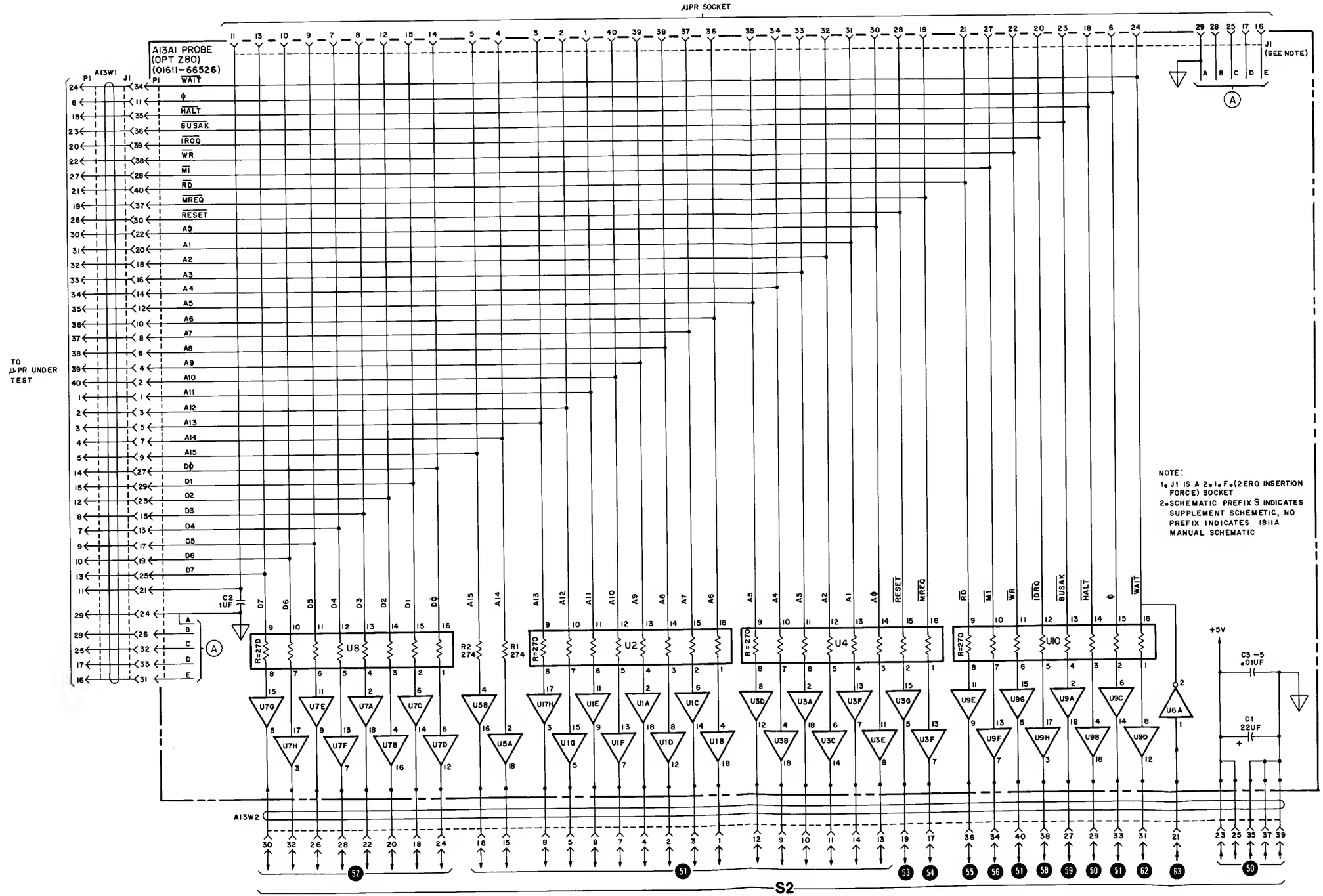
Figure 4-5,
Performance Tests: Replace with figure 7-4.

CHANGE 5

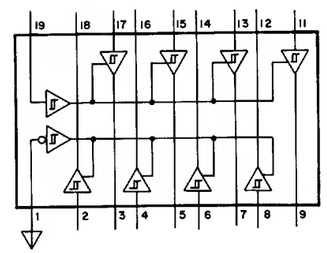
Figure 4-7,
Performance Tests: Replace with figure 7-5.

CHANGE 6

Table 6-1:
A10: Change to HP Part No. 01611-66524.
Add: A10U5, HP Part No. 1816-1106, IC82S181 DEB 5 ROM.
A10U6, HP Part No. 1816-1107, IC82S181 DEB 6 ROM.
A10U7: Change to HP Part No. 1816-1108.
A10U8: Change to HP Part No. 1816-1109.
A10U9: Change to HP Part No. 1816-1114.
A10U10: Change to HP Part No. 1816-1112.
Figure 8-4,
Schematic S4: Replace with figure 7-6.



IC SUPPLY CONFIGURATIONS



ICs ON THIS SCHEMATIC

REF DES	HP PART NO.	MFR PART NO.
U1,3,5,7,9	1820-1918	SN74LS241
U2,4,8,10	1810-0283	
U8	1820-1200	SN74LS05

PARTS ON THIS SCHEMATIC

A13A1
C1-5
R1, 2
U1-10

10260A-001-02-08-77

S1

Figure 7-1.
Replacement for Figure 8-1, Service Sheet S1

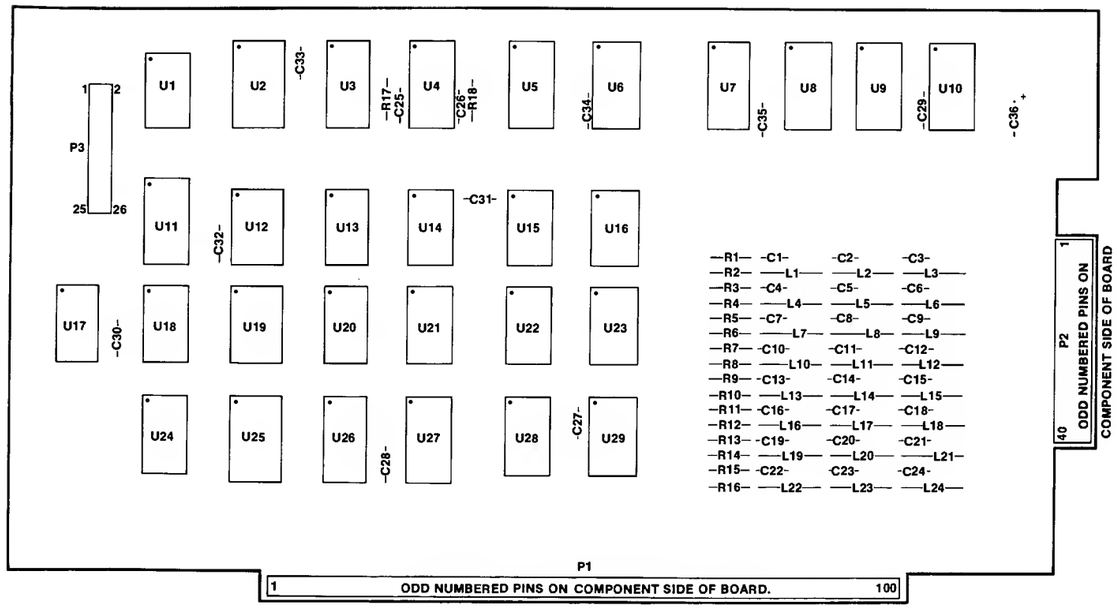


Figure 7-2. Replacement for Figure 8-2, Service Sheets 2A-B (Sheet 1 of 4)

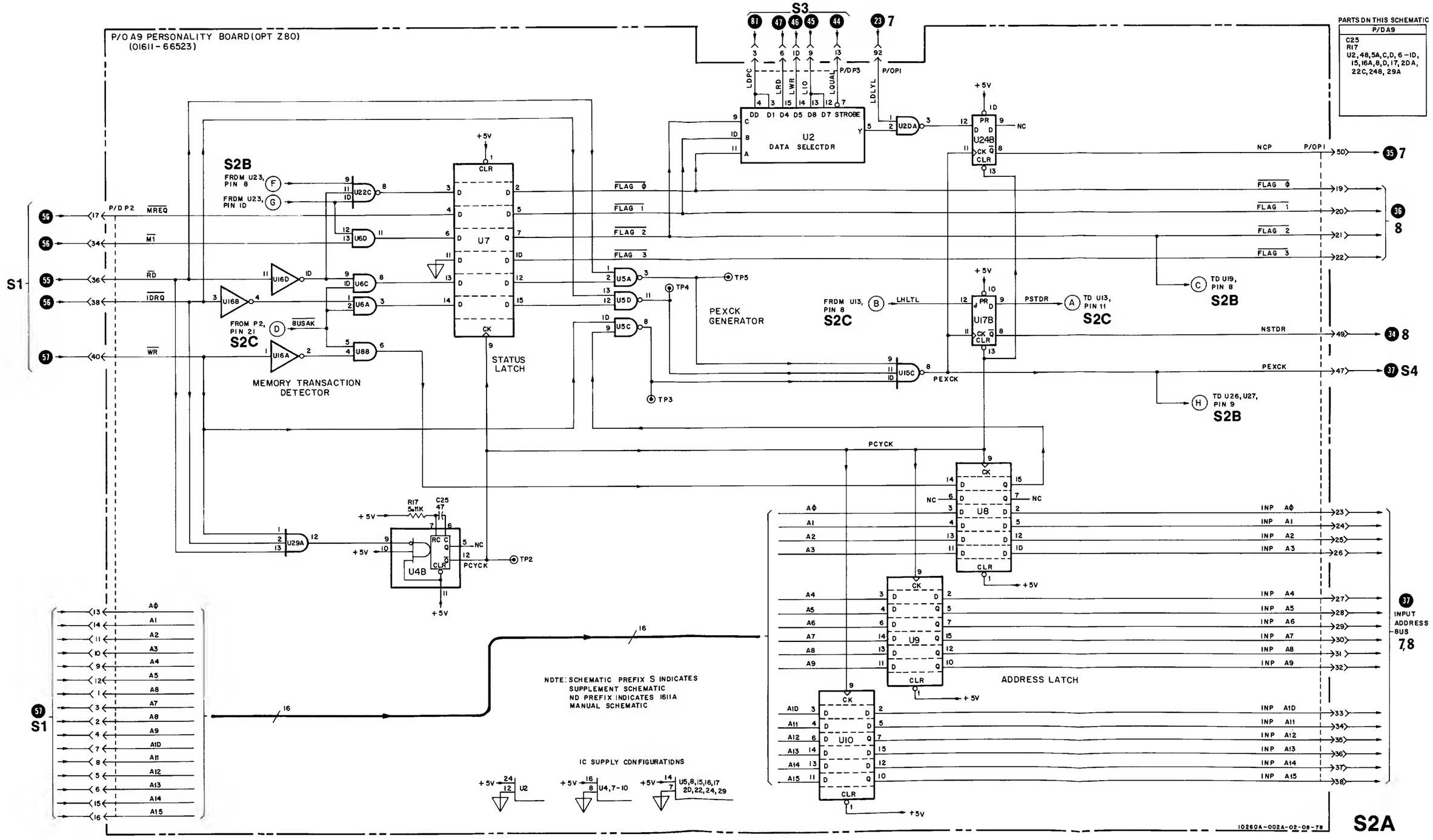


Figure 7-2.
Replacement for Figure 8-2, Service Sheets 2A-B (Sheet 2 of 4)

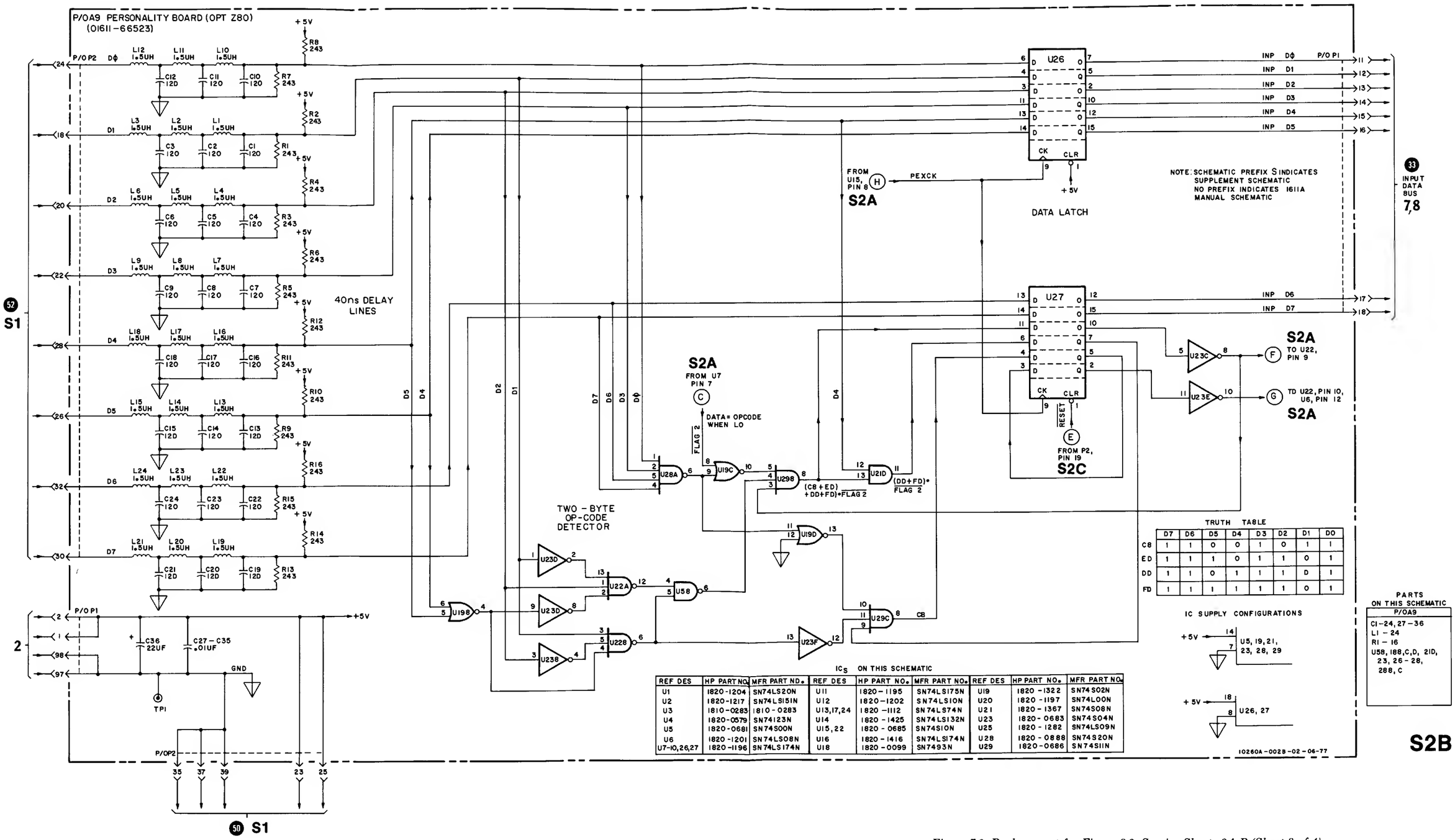


Figure 7-2. Replacement for Figure 8-2, Service Sheets 2A-B (Sheet 3 of 4)

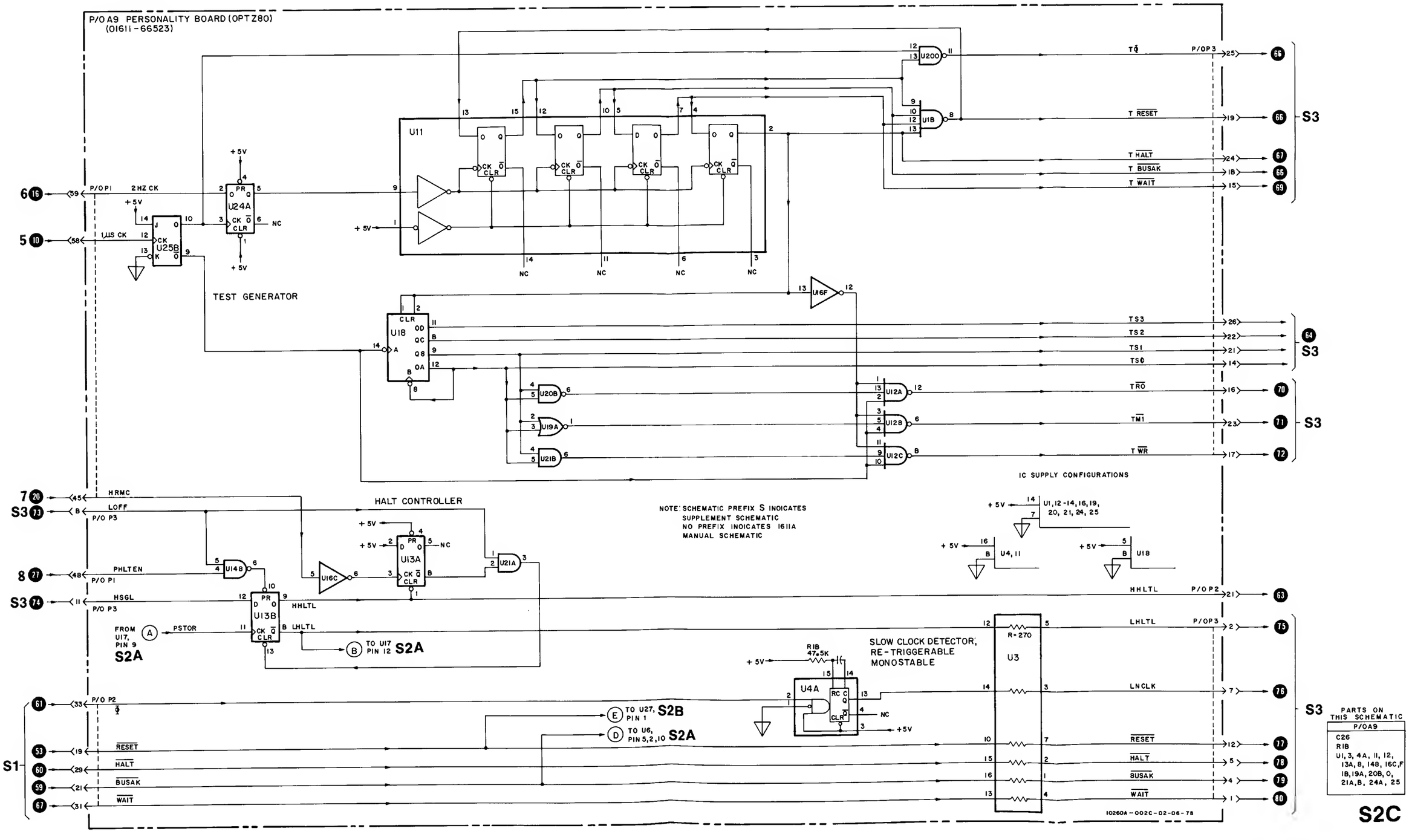


Figure 7-2.
Replacement for figure 8-2, Service Sheets 2A-B (Sheet 4 of 4)

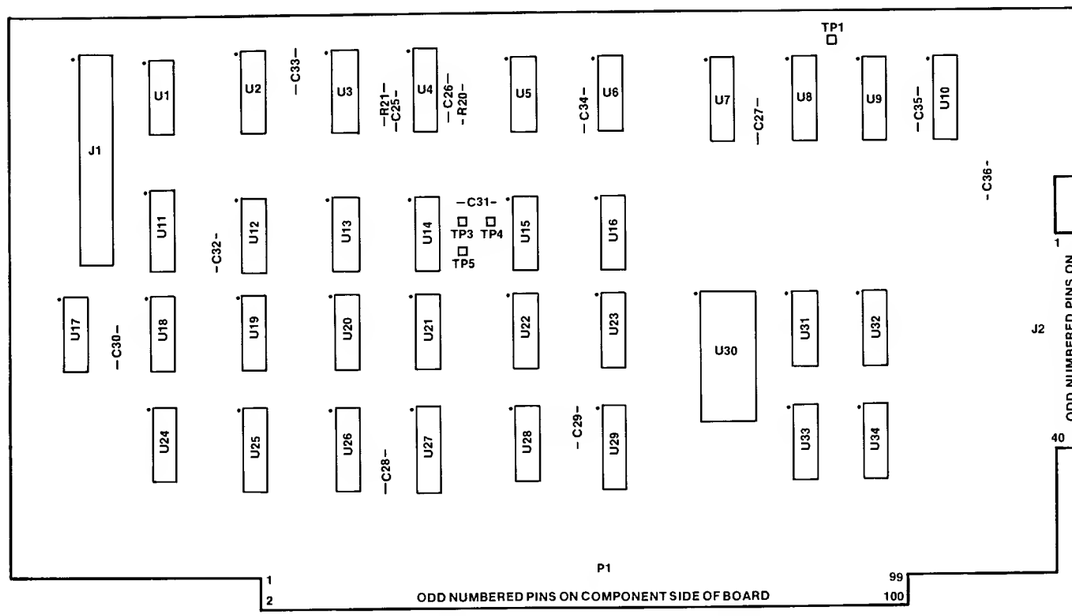
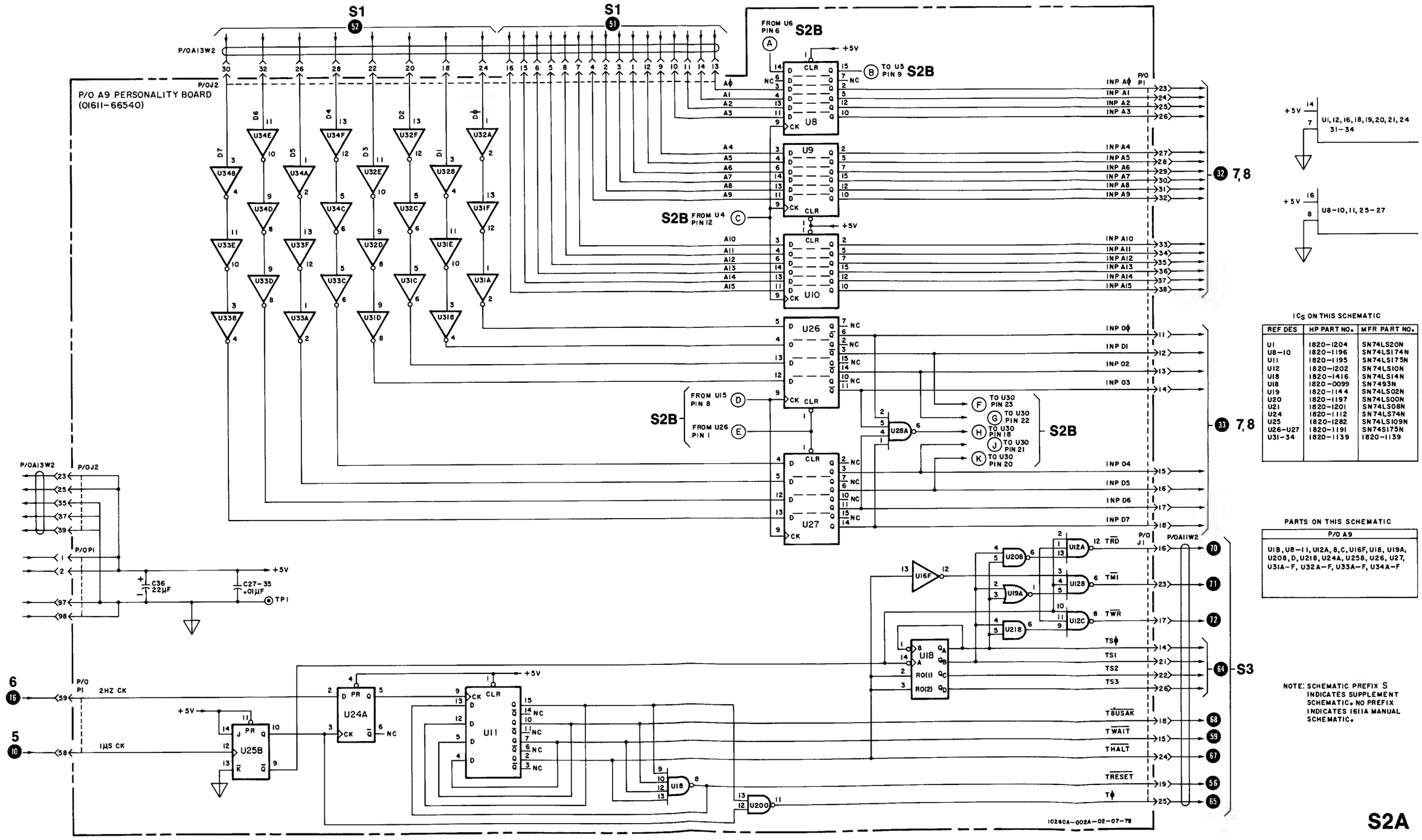


Figure 7-3. Replacement for Figure 8-2, Service Sheets 2A-B (Sheet 1 of 3)



ICs ON THIS SCHEMATIC

REF DES	HP PART NO.	MFR PART NO.
U1	1820-1204	SN74LS20N
U8-10	1820-1196	SN74LS174N
U11	1820-1195	SN74LS175N
U12	1820-1202	SN74LS10N
U18	1820-1416	SN74LS14N
U18	1820-0099	SN7493N
U19	1820-1144	SN74LS02N
U20	1820-1197	SN74LS00N
U21	1820-1201	SN74LS08N
U24	1820-1112	SN74LS74N
U25	1820-1282	SN74LS109N
U26-U27	1820-1191	SN74S175N
U31-34	1820-1139	1820-1139

PARTS ON THIS SCHEMATIC

P/O A9
U1B, U8-11, U12A, B, C, U16F, U18, U19A, U20B, D, U21B, U24A, U25B, U26, U27, U31A-F, U32A-F, U33A-F, U34A-F

NOTE: SCHEMATIC PREFIX S INDICATES SUPPLEMENT SCHEMATIC. NO PREFIX INDICATES 1611A MANUAL SCHEMATIC.

Figure 7-3.
Replacement for Figure 8-2, Service Sheets 2A-B (Sheet 2 of 3)

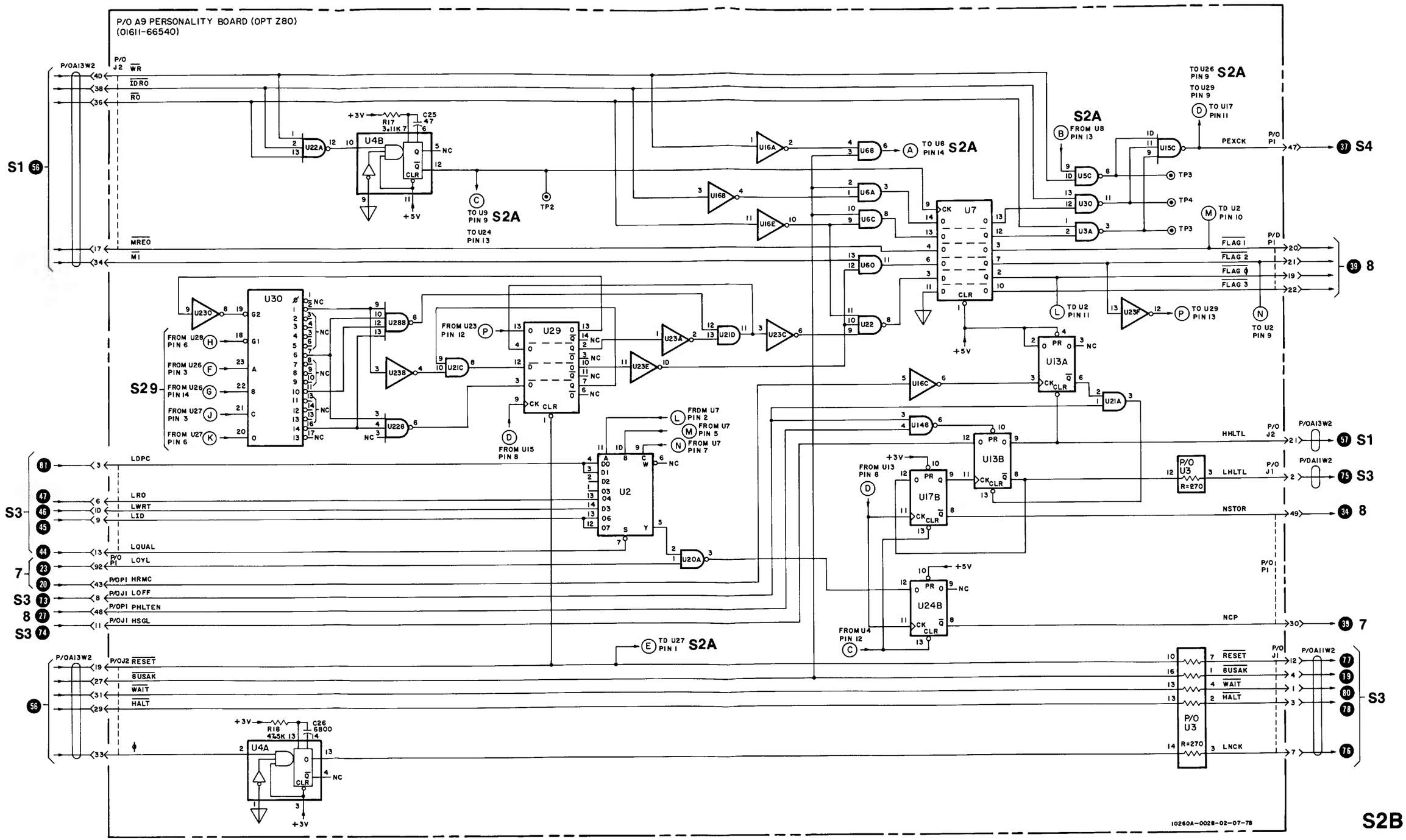


Figure 7-3. Replacement for Figure 8-2, Service Sheets 2A-B (Sheet 3 of 3)

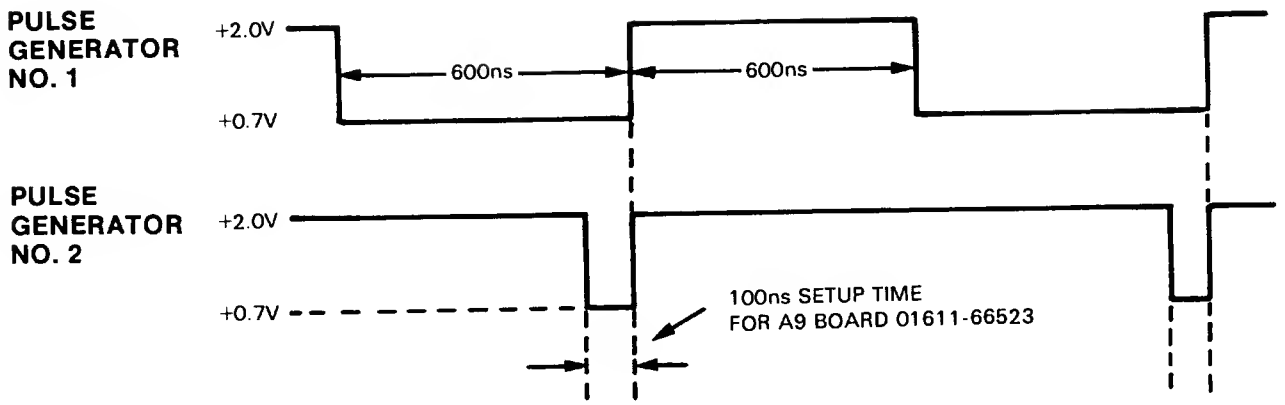


Figure 7-4. Replacement for Figure 4-5, Data Lines Test Waveforms

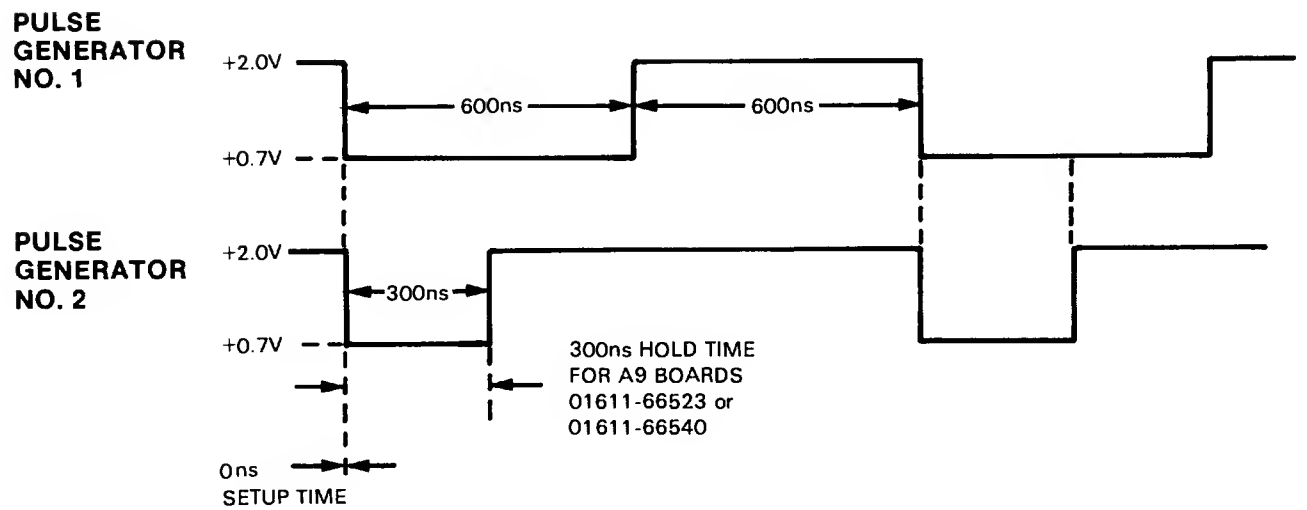


Figure 7-5. Replacement for Figure 4-7, Address Line Test Waveforms

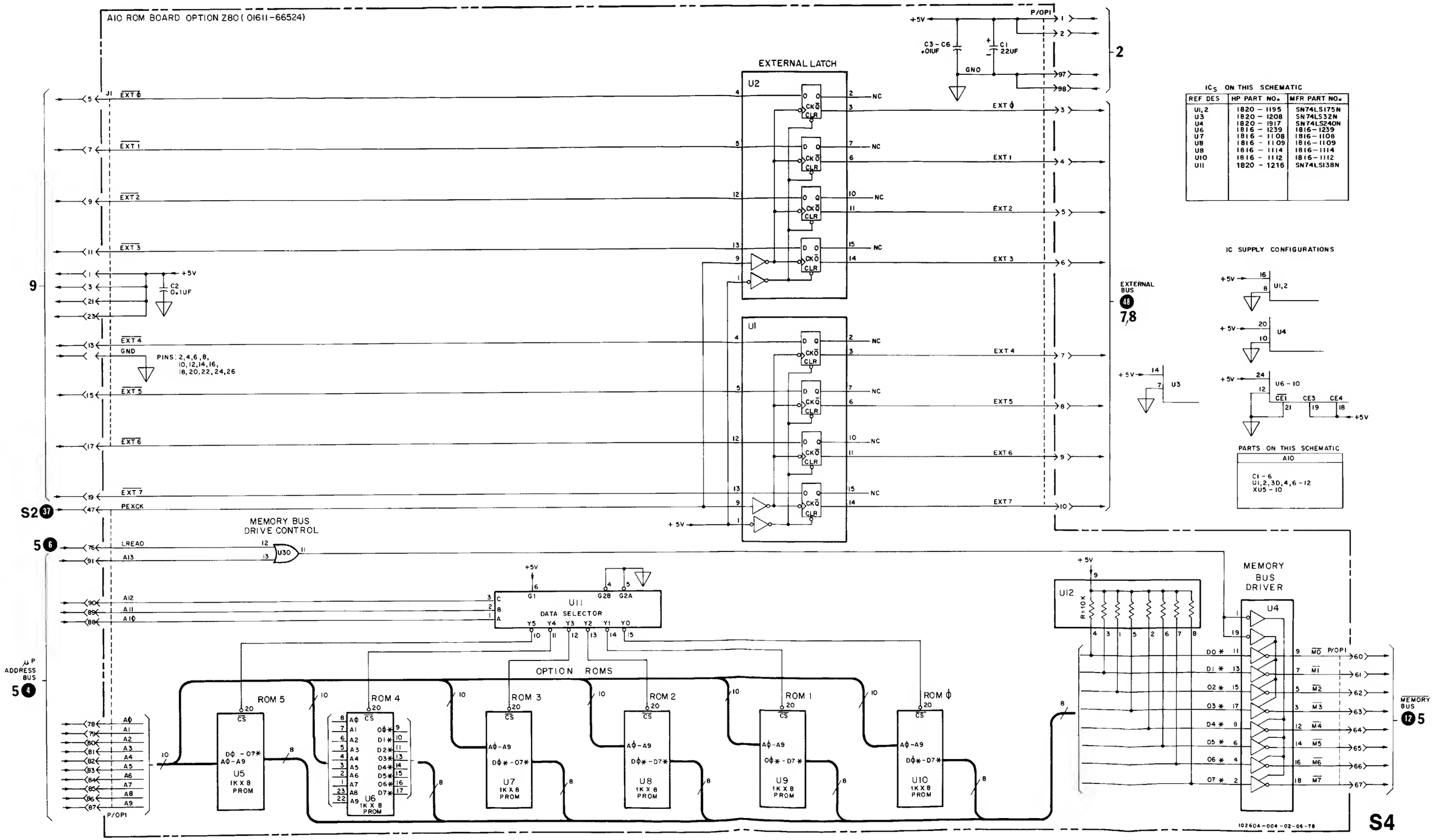


Figure 7-6.
Replacement for Figure 8-4 Service Sheet 4, ROM Board A10 (Sheet 2 of 2)
7-13/(7-14 blank)

SECTION VIII

SERVICE

8-1. INTRODUCTION.

8-2. This section contains the schematic diagrams for the Model 10260A/1611A Option Z80.

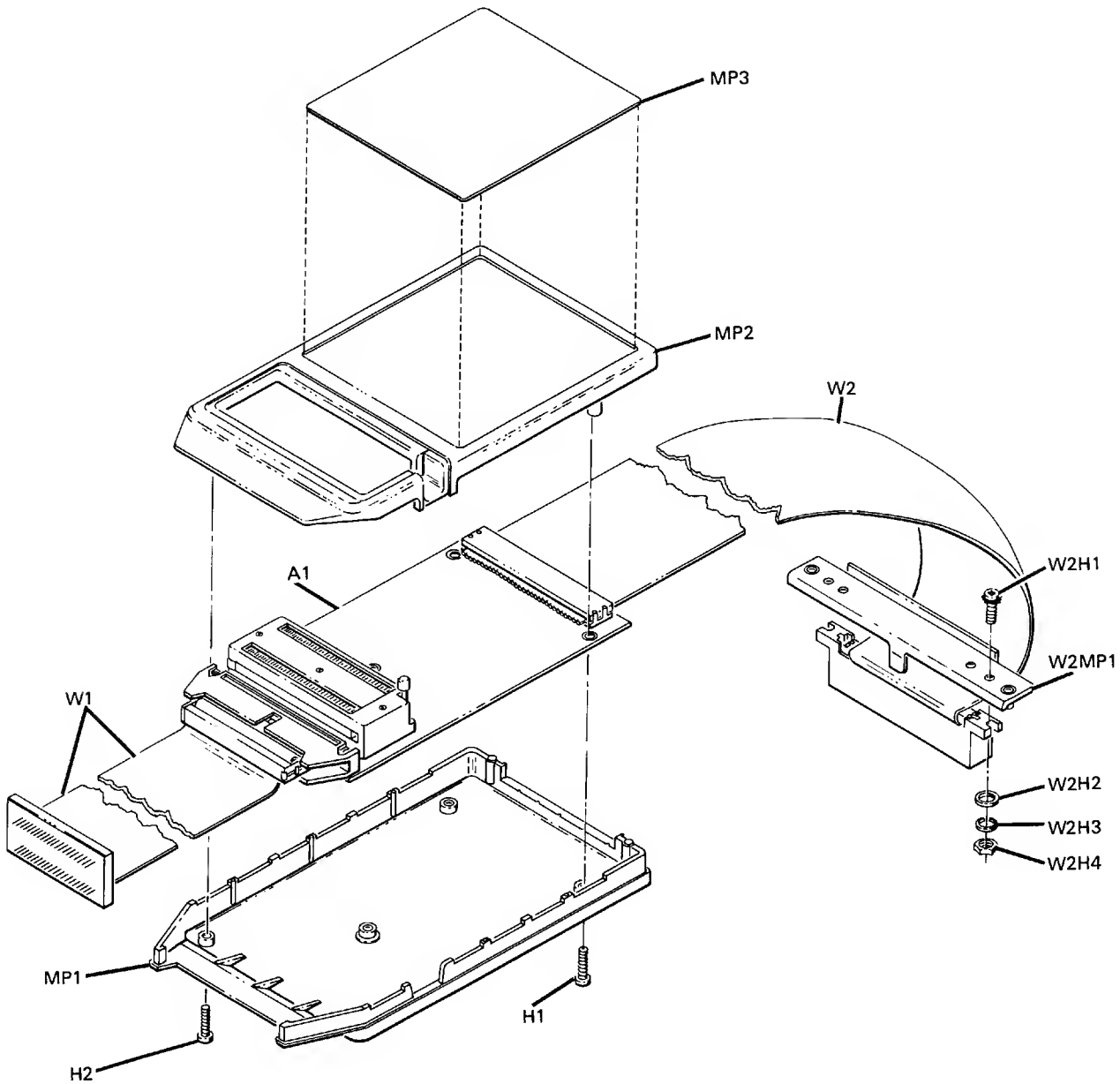
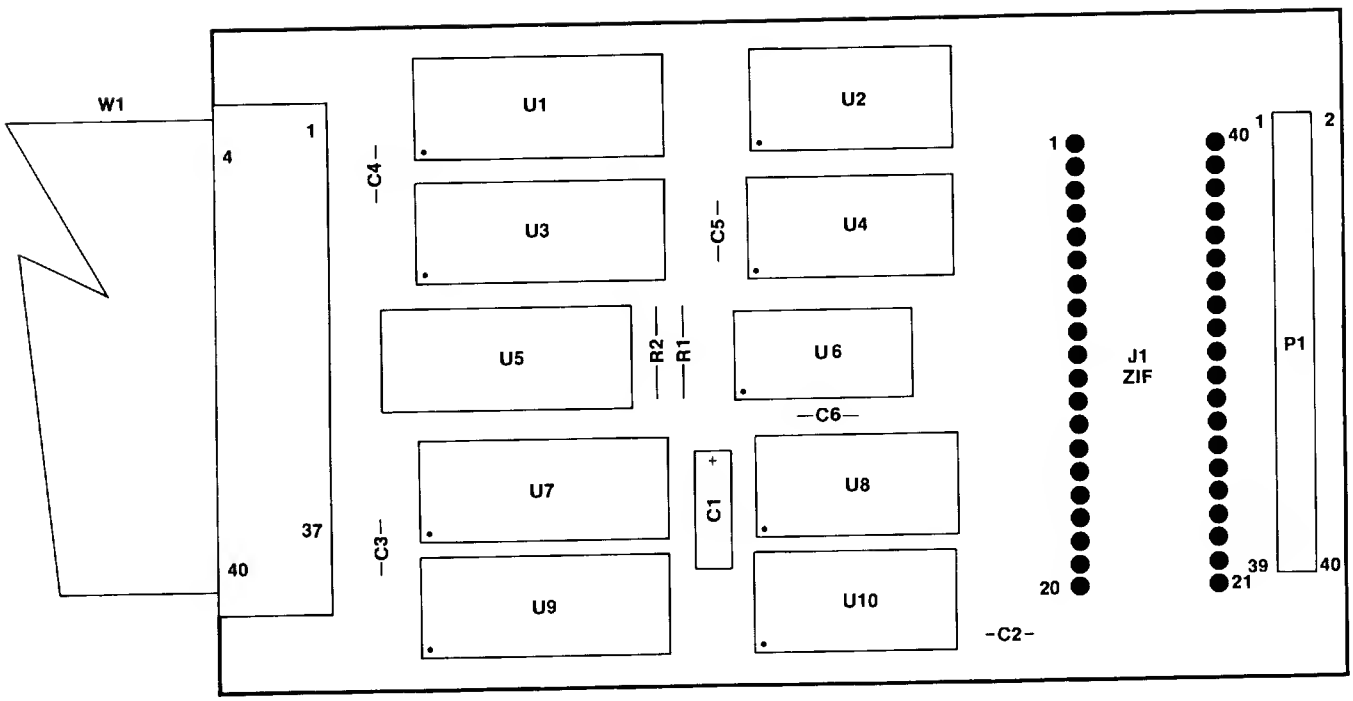


Figure 8-1. Service Sheet 1, Microprocessor Probe A13 (Sheet 1 of 3)



A13A1 Component Location (01611-66541)

Figure 8-1. Service Sheet 1, Microprocessor Probe A13 (Sheet 2 of 3)

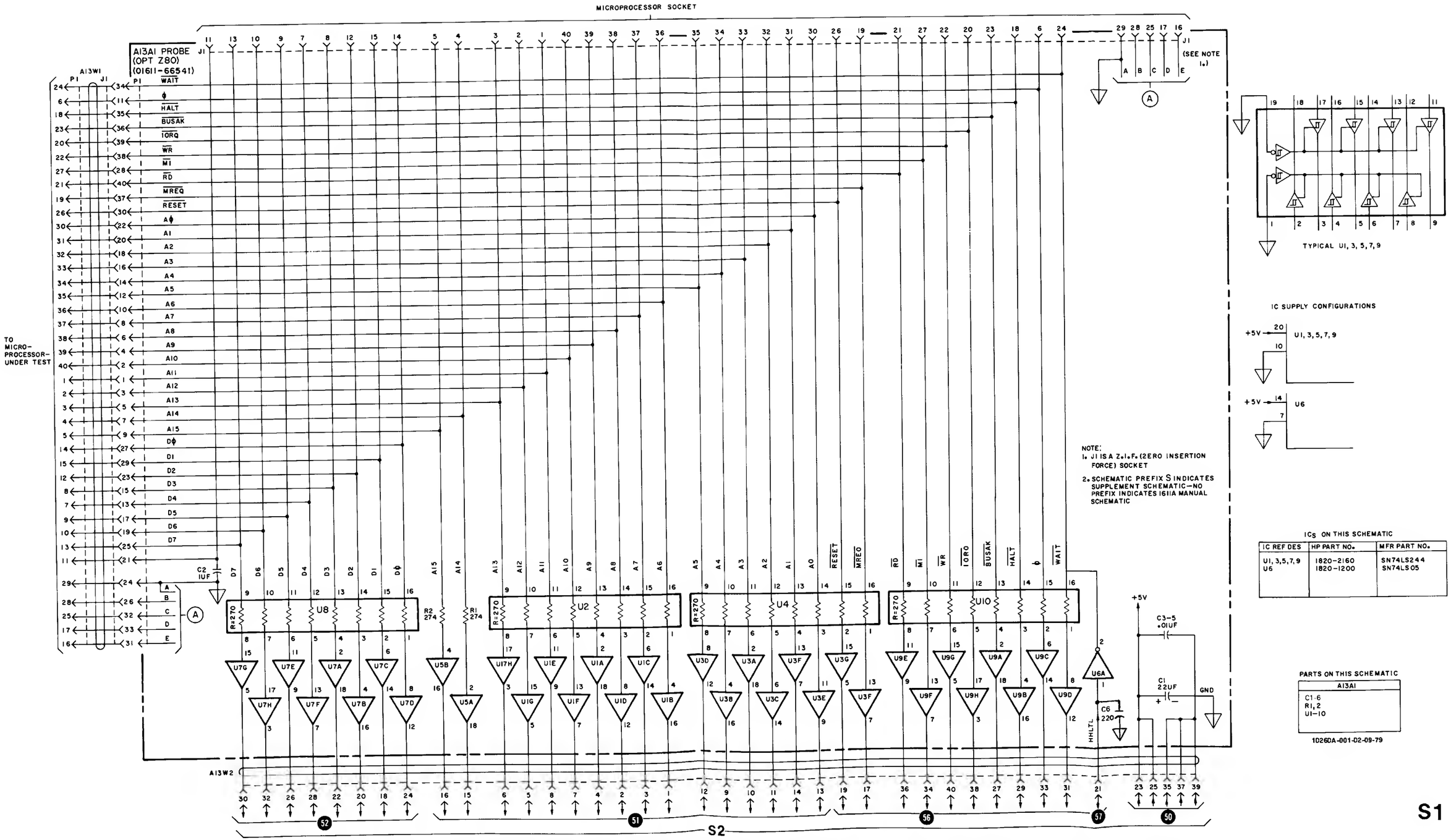
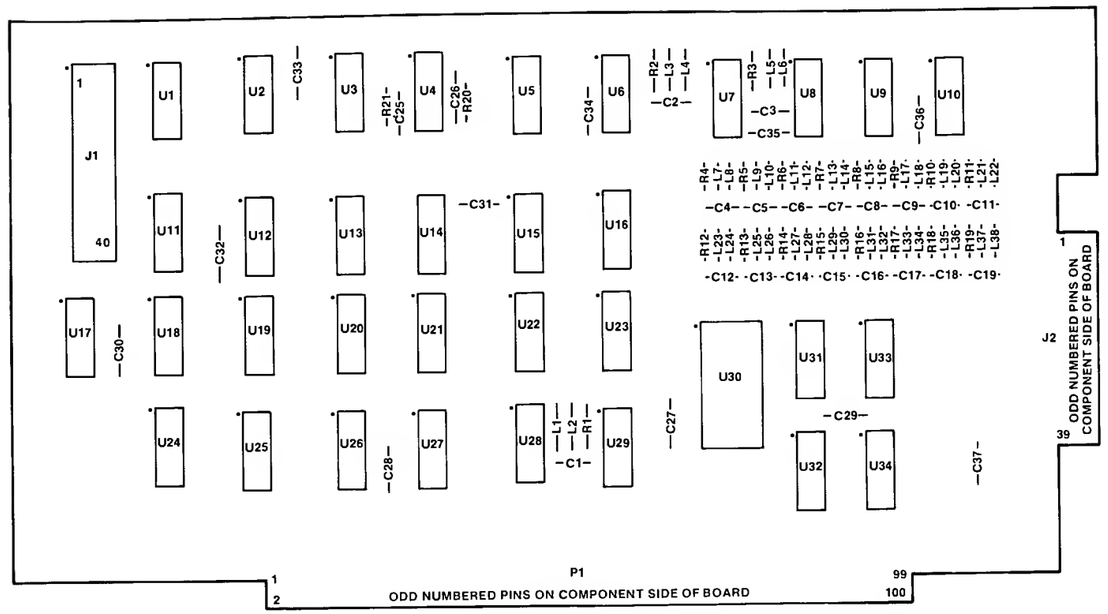
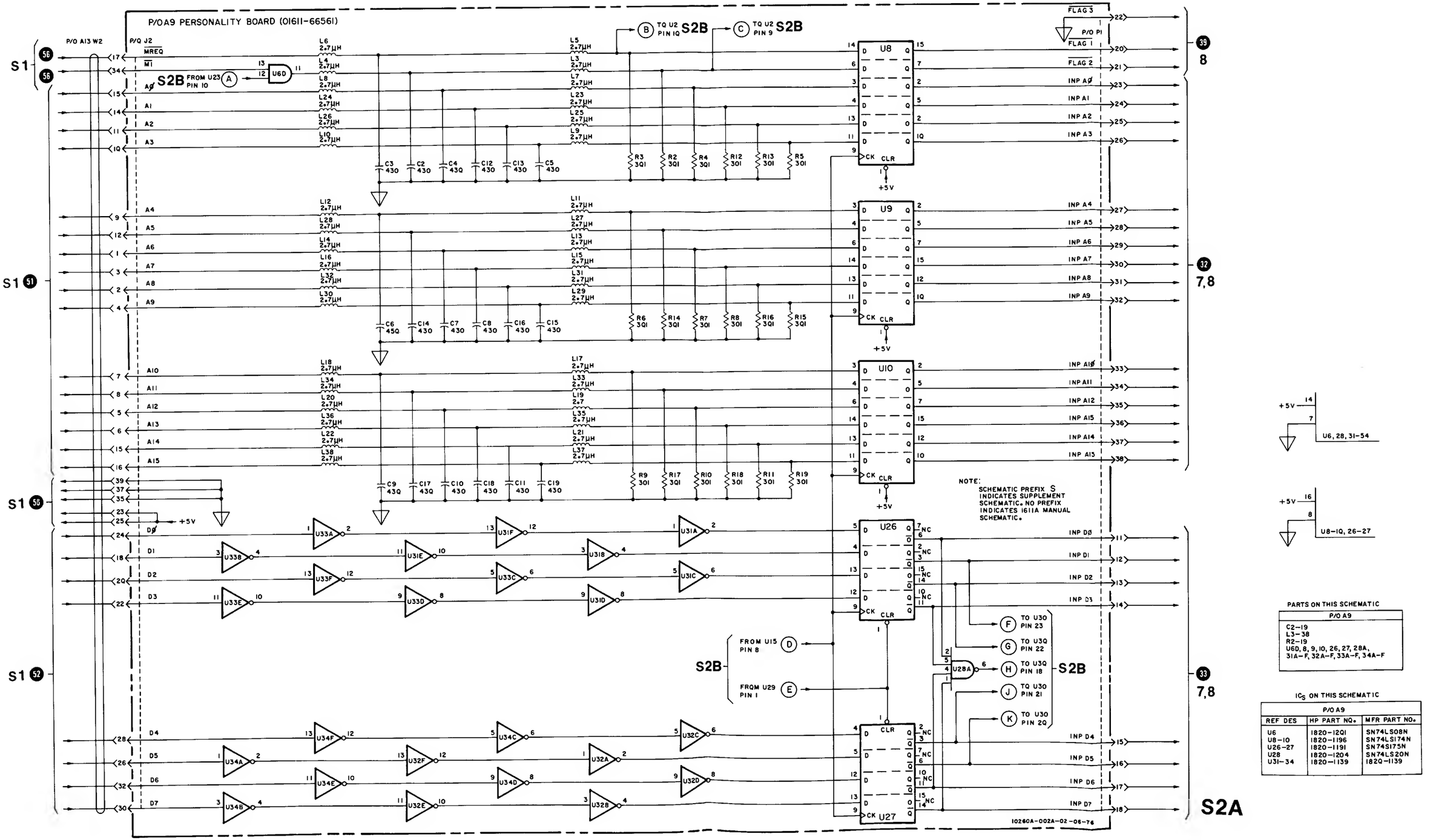


Figure 8-1.
Service Sheet 1, Microprocessor Probe A13 (Sheet 3 of 3)



A9 Component Location (01611-66561)

Figure 8-2. Service Sheet 2, Personality Board A9, (Sheet 1 of 4)



PARTS ON THIS SCHEMATIC

P/O A9
C2-19 L3-38 R2-19 U6D, 8, 9, 10, 26, 27, 28A, 31A-F, 32A-F, 33A-F, 34A-F

ICs ON THIS SCHEMATIC

P/O A9		
REF DES	HP PART NO.	MFR PART NO.
U6	1820-1201	SN74LS08N
U8-10	1820-1196	SN74LS174N
U26-27	1820-1191	SN74S175N
U28	1820-1204	SN74LS20N
U31-34	1820-1139	1820-1139

Figure 8-2.
Service Sheet 2, Personality Board A9, (Sheet 2 of 4)

ICs ON THIS SCHEMATIC

IC REF DES	HP PART NO.	MFR PART NO.
U1, 28	1820-1204	SN74LS20N
U2	1820-1217	SN74LS151N
U4	1820-0579	SN74123N
U5	1820-1307	SN74S132N
U6, 21	1820-1201	SN74LS08N
U7, 29	1820-1196	SN74LS174N
U11	1820-1195	SN74LS175N
U12, 22	1820-1202	SN74LS10N
U13, 17, 24	1820-1112	SN74LS74N
U14	1820-1425	SN74LS132N
U15	1820-0685	SN74S10N
U16	1820-1416	SN74LS14N
U18	1820-0099	SN7493N
U19	1820-1144	SN74LS02N
U20	1820-1197	SN74LS00N
U23	1820-1199	SN74LS04N
U25	1820-1282	SN74LS109N
U30	1820-0495	SN74154N

PARTS ON THIS SCHEMATIC

P/O A9
C1, 25-26 L1-2 R1, 17-18 U1B, 2, 3, 4A-B, 5A, C-D, 6A-C, 7, 11, 12A-C, 13A-B, 14B-C, 15C, 16A-C, E-F, 17B, 18, 19A, 20A-B, D, 21A-D, 22A-C, 23A-F, 24A-B, 25B, 28B, 29, 30

Figure 8-2. Service Sheet 2, Personality Board A9, (Sheet 3 of 4)

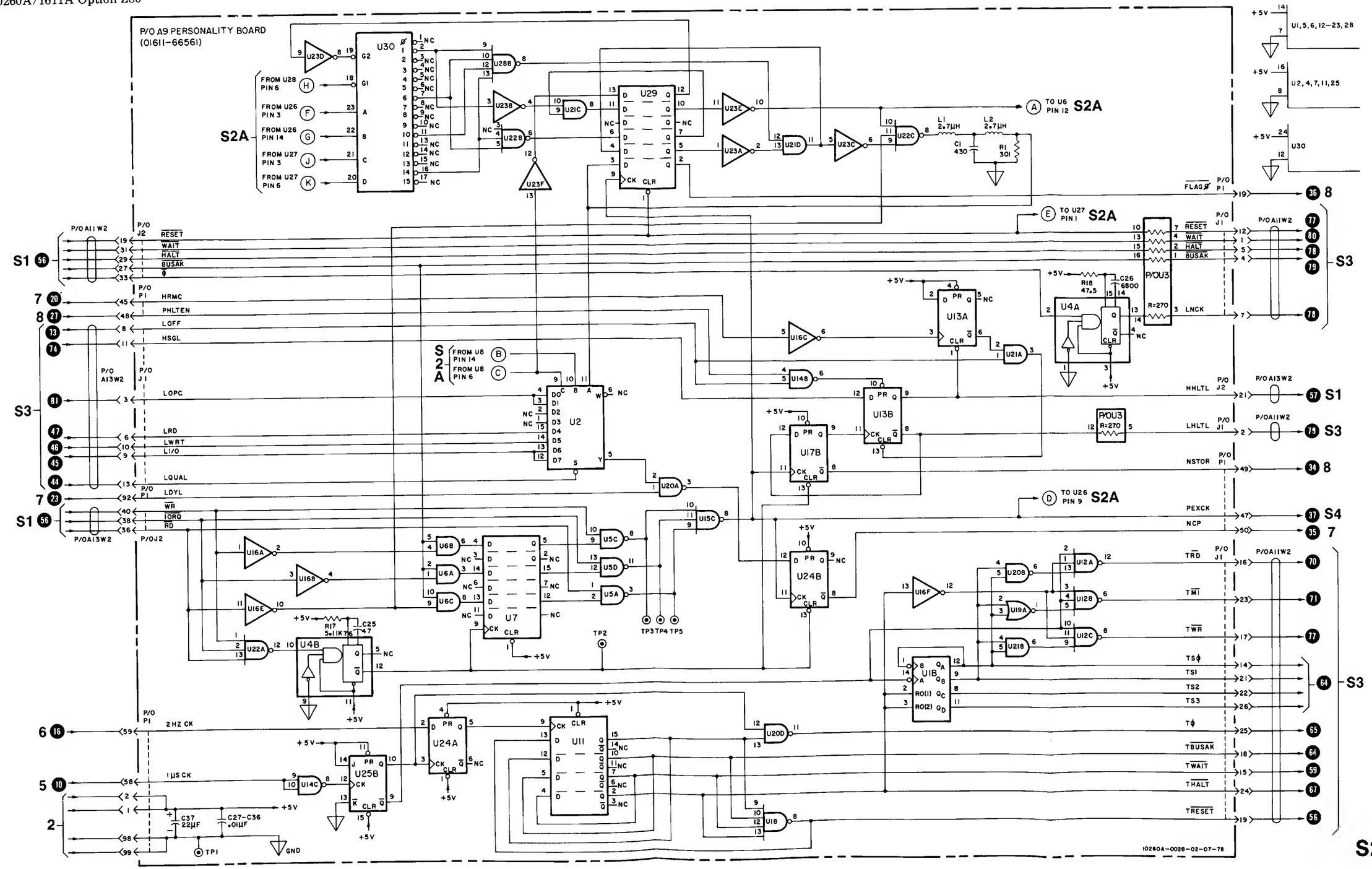
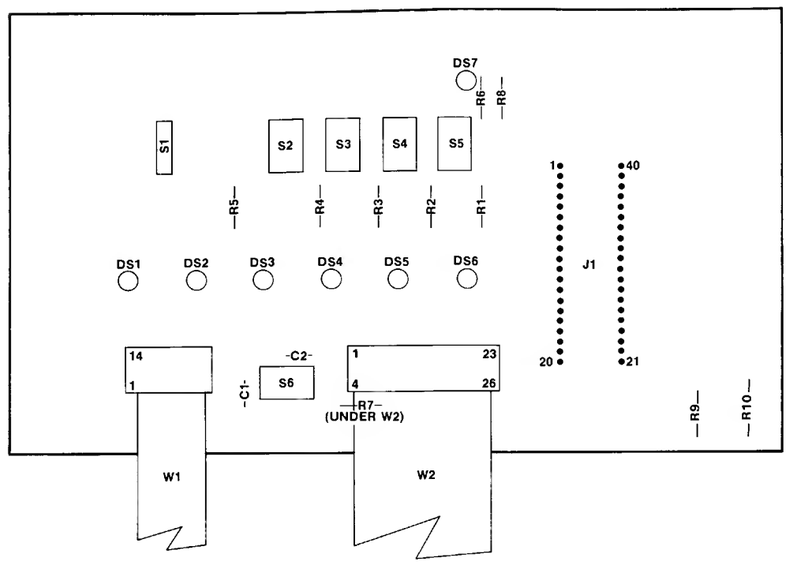


Figure 8-2.
Service Sheet 2, Personality Board A9, (Sheet 4 of 4)
8-7



A11A1 Component Location (01611-66573)

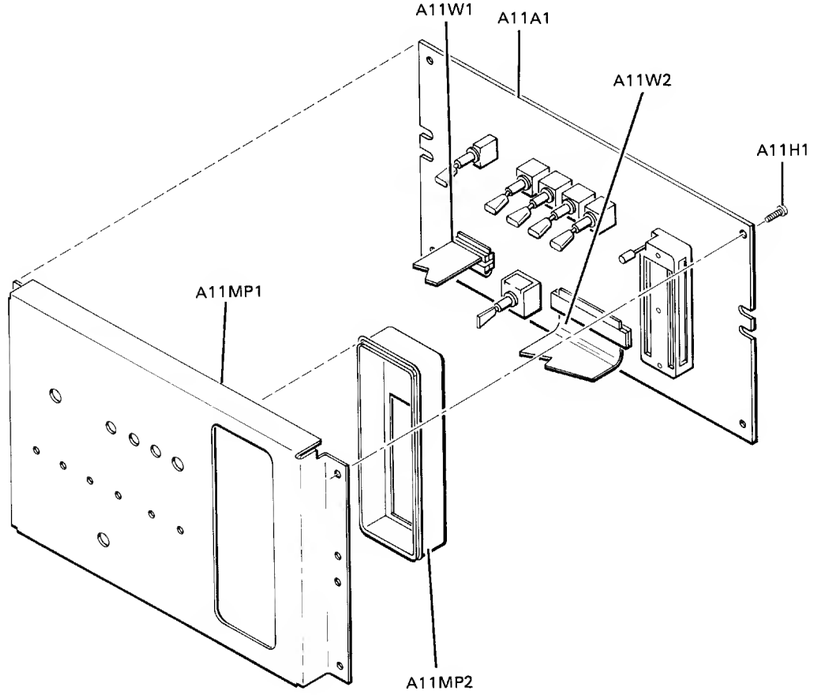


Figure 8-3. Service Sheet 3, Personality Panel A11 (Sheet 1 of 2)

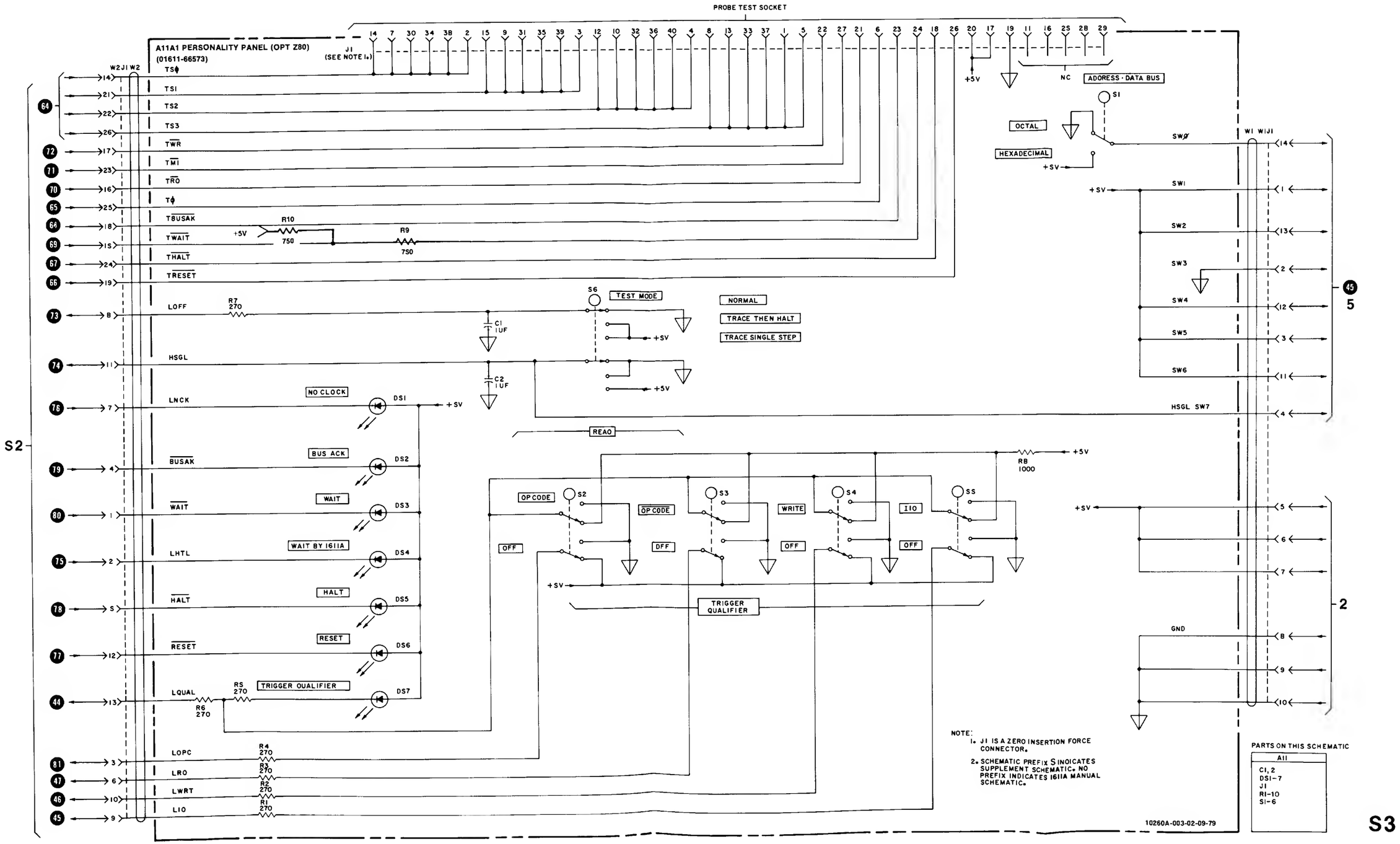
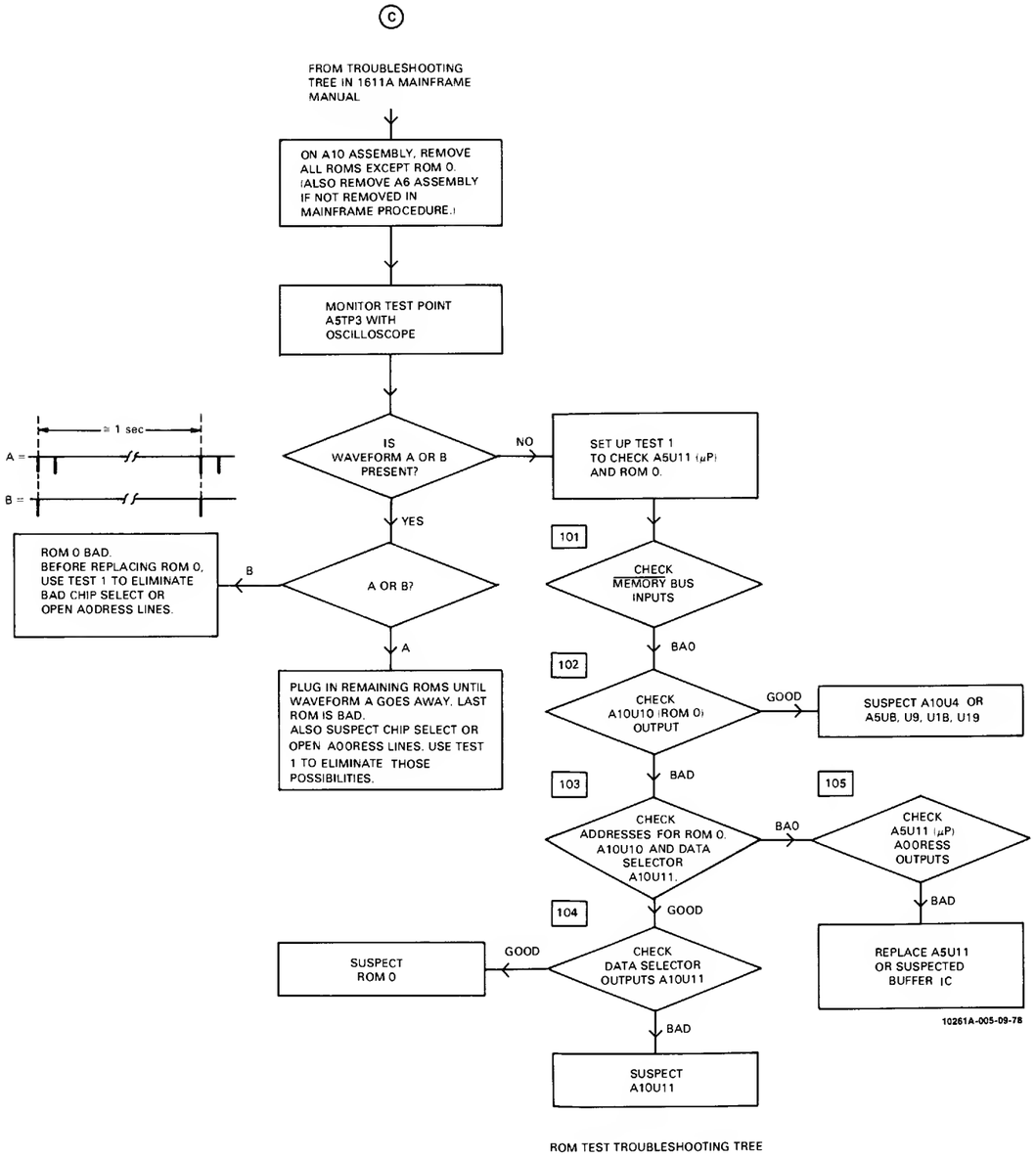
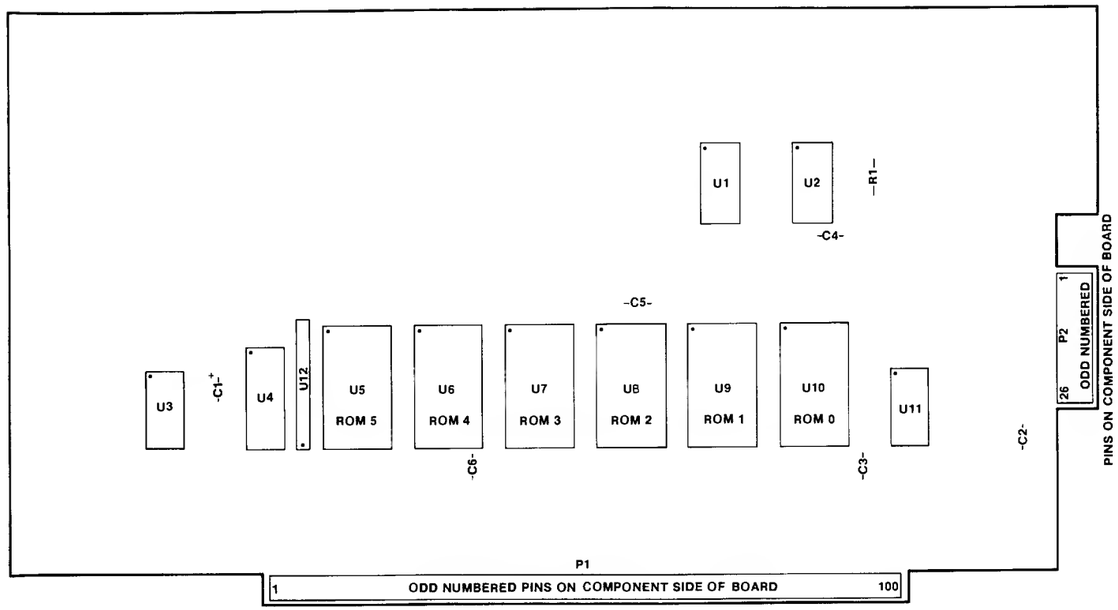


Figure 8-3.
Service Sheet 3, Personality Panel A11A1 (Sheet 2 of 2)



ROM TEST TROUBLESHOOTING TREE



A10 Component Location (01611-66568)

A10 TROUBLESHOOTING

An HP 5004A Signature Analyzer may be used to troubleshoot the A10 Assembly. With this technique, the internal microprocessor in the 1611A, A5U11, is forced to increment through the complete address range of 0000_{16} to $FFFF_{16}$. The 1611A now addresses all locations in ROM 0 and the 5004A can verify the data contents of memory (ROM 0) and also verify proper operation of the address lines from the 1611A microprocessor.

Figure 8-4. Service Sheet 4, ROM Board A10 (Sheet 1 of 4)

SIGNATURE ANALYSIS PROCEDURE NO. 1.

a. Set 1611A LINE switch to off position.

b. Remove A6, A7, A9, and A10 boards from 1611A.

c. Reinstall A10 Board on extender board A14.

d. Ground A5U3 pin 6 and A5U11 pin 6.

e. Connect signature analyzer probes to the following circuit points.

START ..... A5U11, Pin 36
STOP ..... A5U11, Pin 38
CLOCK ..... A5U11, Pin 17
GND ..... A5TP (GND)

f. Set signature analyzer controls as follows:

START .....
STOP .....
CLOCK .....

g. Set 1611A LINE switch to on position.

h. Verify that signatures called out in troubleshooting tree match the following table.

MEASUREMENT NUMBER	TEST POINTS	SIGNATURES	
	A10 boards 01611-66524 and 01611-66568	**A10 board 01611-66524**	**A10 board 01611-66568**
101	V_H	P254	P254
	A5U8, pin 5	A8PF	U85F
	A5U8, pin 1	UPAF	131F
	A5U8, pin 9	AOUA	31CH
	A5U8, pin 13	314F	C160
	A5U9, pin 5	C583	P5FP
	A5U9, pin 1	600F	H35A
	A5U9, pin 9	A220	9HU9
	A5U9, pin 13	CH06	5124
102	A10U10, pin 9	4AC8	1A08
	A10U10, pin 10	1FU8	U148
	A10U10, pin 11	42AP	H39P
	A10U10, pin 13	H318	5334
	A10U10, pin 14	57H7	079A
	A10U10, pin 15	8258	310P
	A10U10, pin 16	4074	7UAH
	A10U10, pin 17	5U52	C370
	A10 board 01611-66524 and 01611-66568	**A10 board 01611-66524**	**A10 board 01611-66568**
103	A10U10, pin 8	5P33	5P33
	A10U10, pin 7	FA11	FA11
	A10U10, pin 6	3HUA	3HUA
	A10U10, pin 5	12U0	12U0
	A10U10, pin 4	C7A5	C7A5
	A10U10, pin 3	46HC	46HC
	A10U10, pin 2	65CA	65CA
	A10U10, pin 1	8AUC	8AUC
	A10U10, pin 23	9241	9241
	A10U10, pin 22	1U5P	1U5P
	A10U11, pin 1	AAHU	U665
	A10U11, pin 2	U665	826P
	A10U11, pin 3	826P	0000

Figure 8-4. Service Sheet 4, ROM Board A10 (Sheet 2 of 4)

MEASUREMENT NUMBER	TEST POINTS	SIGNATURES	
	A10 boards 01611-66524 and 01611-66568	**A10 board 01611-66524**	**A10 board 01611-66568**
104	A10U11, pin 15	879F	OP7C
	A10U11, pin 14	6CC3	6P41
	A10U11, pin 13	931U	1A4A
	A10U11, pin 12	1UOA	not used
	A10U11, pin 11	4A78	not used
	A10 ROM boards 01611-66524 and 01611-66568	**A10 ROM boards 01611-66524 and 01611-66568**	
105	A5U21C, pin 7	5P33	
	A5U21C, pin 6	5P33	
	A5U21B, pin 5	FA11	
	A5U21B, pin 4	FA11	
	A5U21A, pin 3	3HUA	
	A5U21A, pin 2	3HUA	
	A5U21D, pin 9	12UO	
	A5U21D, pin 10	12UO	
	A5U21E, pin 11	C7A5	
	A5U21E, pin 12	C7A5	
	A5U12E, pin 11	65CA	
	A5U12E, pin 12	65CA	
	A5U12F, pin 13	8AUC	
	A5U12F, pin 14	8AUC	
	A5U12C, pin 7	9241	
	A5U12C, pin 6	9241	
	A5U12B, pin 5	1U5P	
	A5U12B, pin 4	1U5P	
	A5U2B, pin 6	AAHU	
	A5U2B, pin 5	AAHU	
	A5U2A, pin 3	U665	
	A5U2A, pin 2	U665	
	A5U12A, pin 3	826P	
	A5U12A, pin 2	826P	
	A5U2C, pin 8	VLP	
	A5U2C, pin 9	VLP	
		VLP = 0000	

Figure 8-4. Service Sheet 4, ROM Board A10 (Sheet 3 of 4)

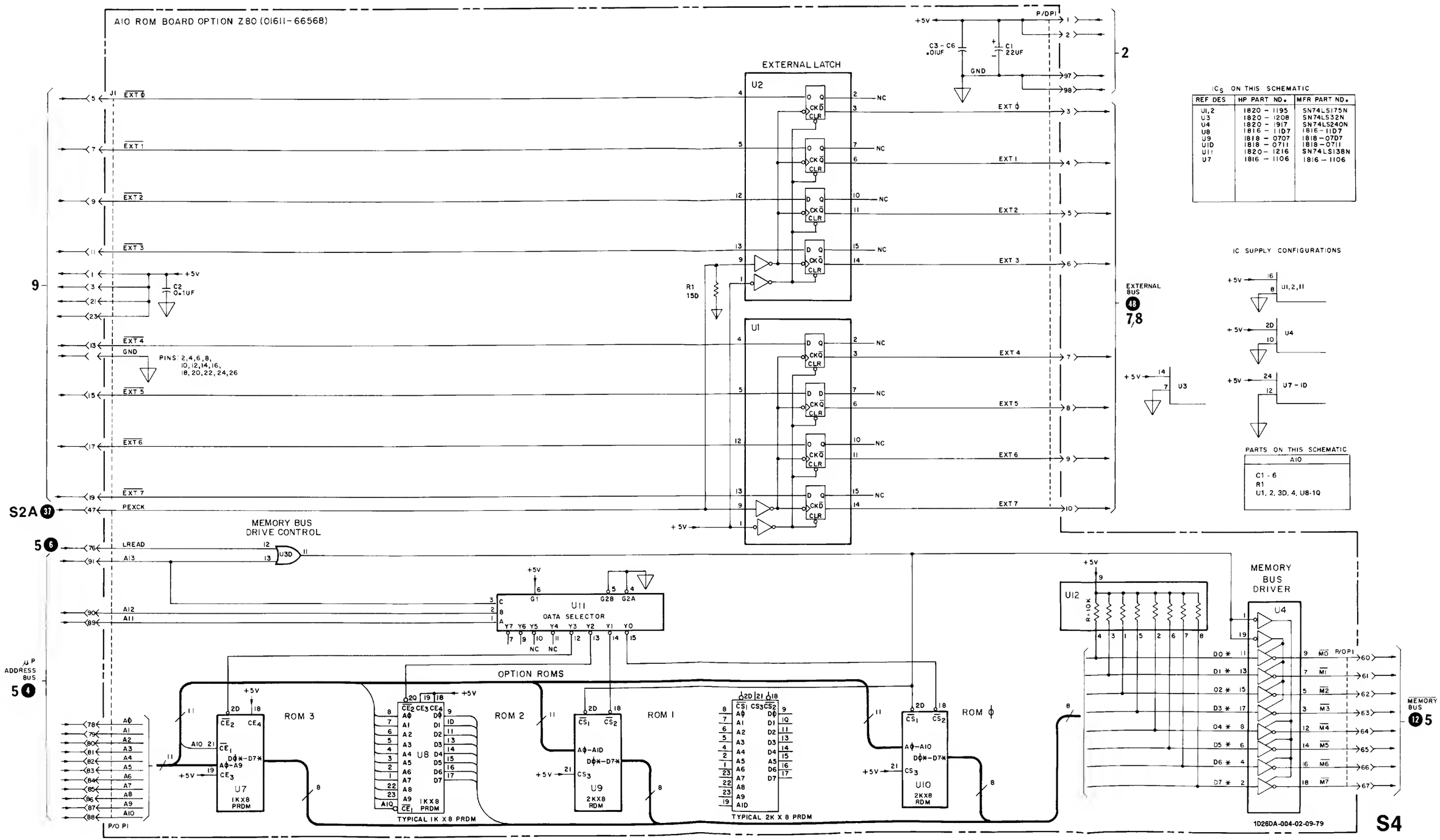


Figure 8-4.
Service Sheet 4, ROM Board A10 (Sheet 4 of 4)

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